

Computer Architecture

Week 1: Introduction



Fenerbahçe University

Professor & TAs

Prof: Dr. Vecdi Emre Levent

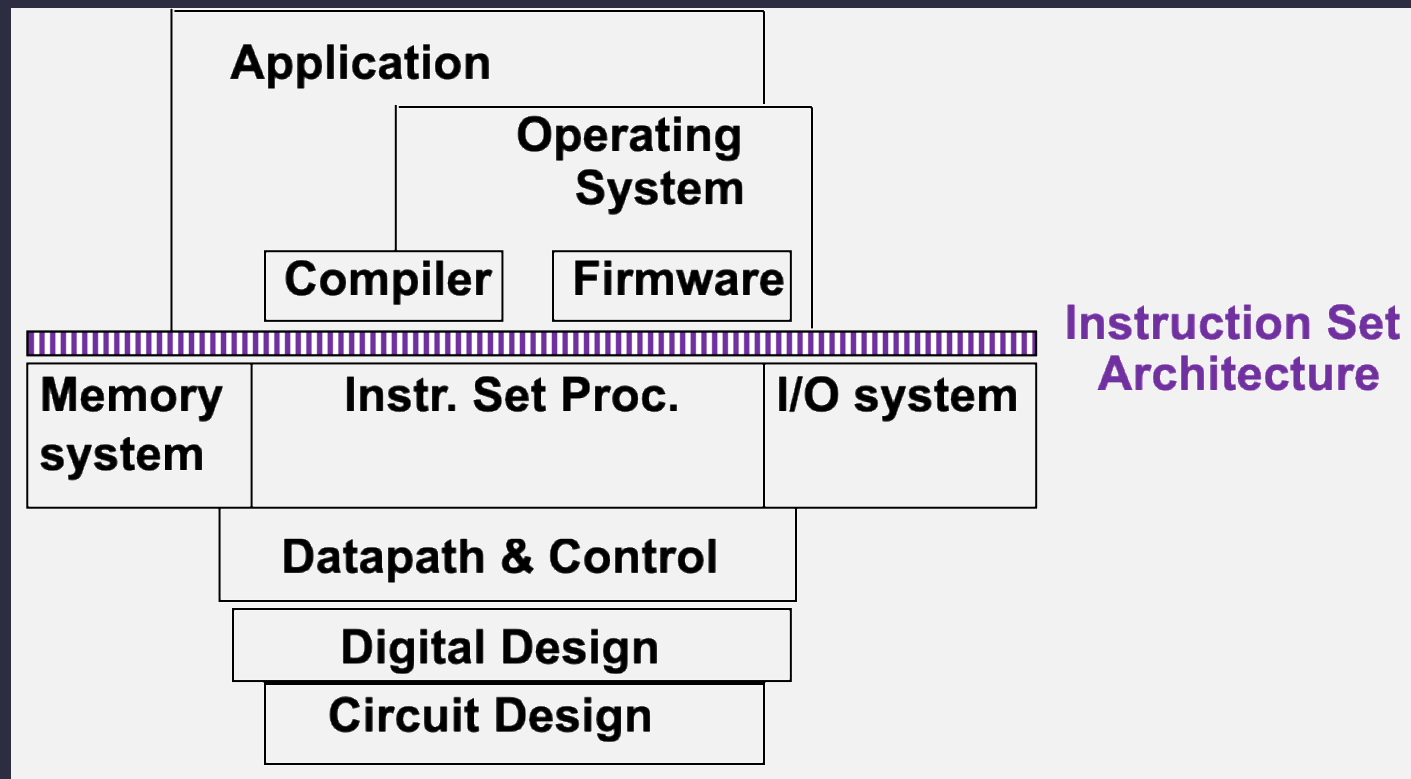
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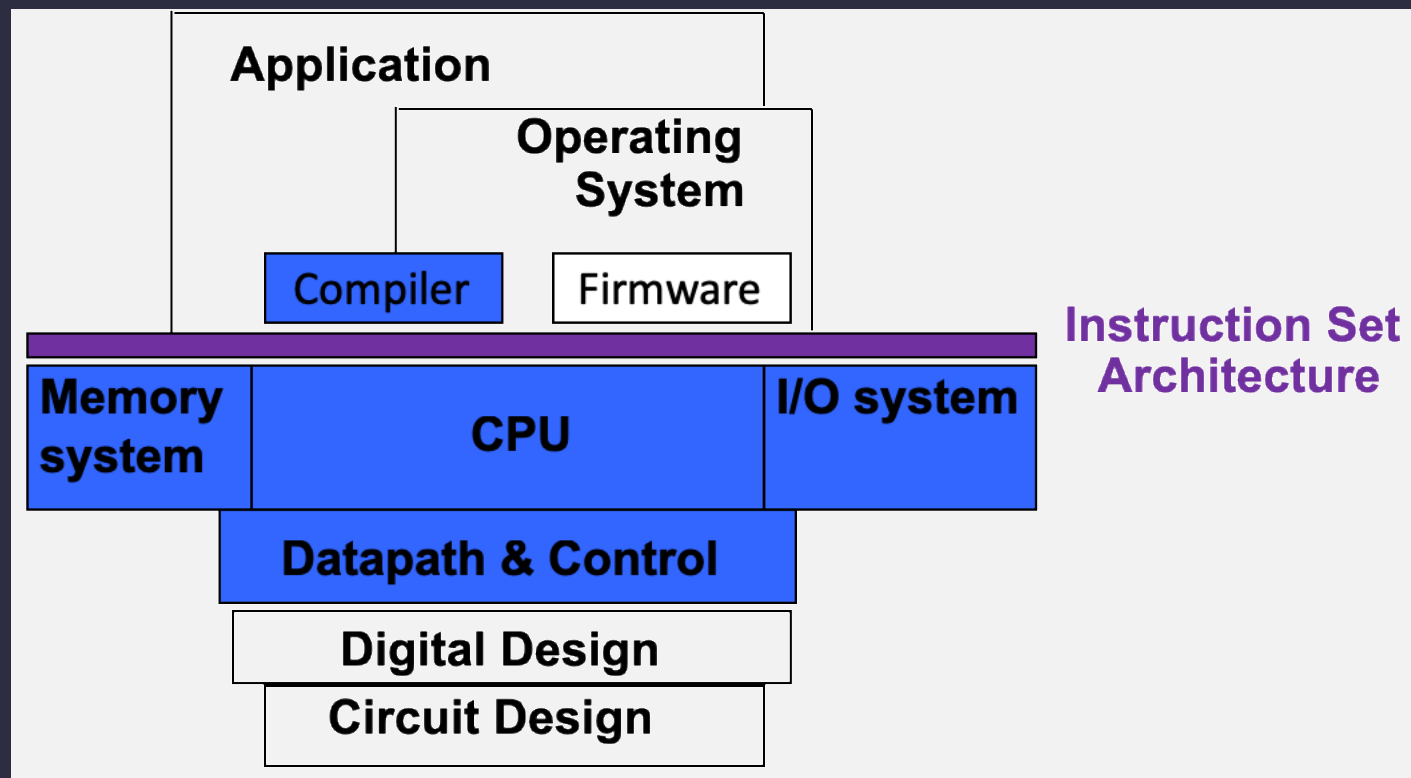
Course Plan

- Computer Architecture
 - Introduction
 - Logic Gates & Arithmetic
 - Combinational and Sequential Circuits
 - Finite State Machines
 - Memories
 - RISC-V Processor
 - Pipelining and Performance
 - RISC-V Processor Design
 - RISC, CISC, ISA and Callings
 - Assembler, Linker and Loader
 - Caches
 - Virtual Memory, System Calls and Interrupts
 - Parallelism, Multicore and Synchronisation

Brief

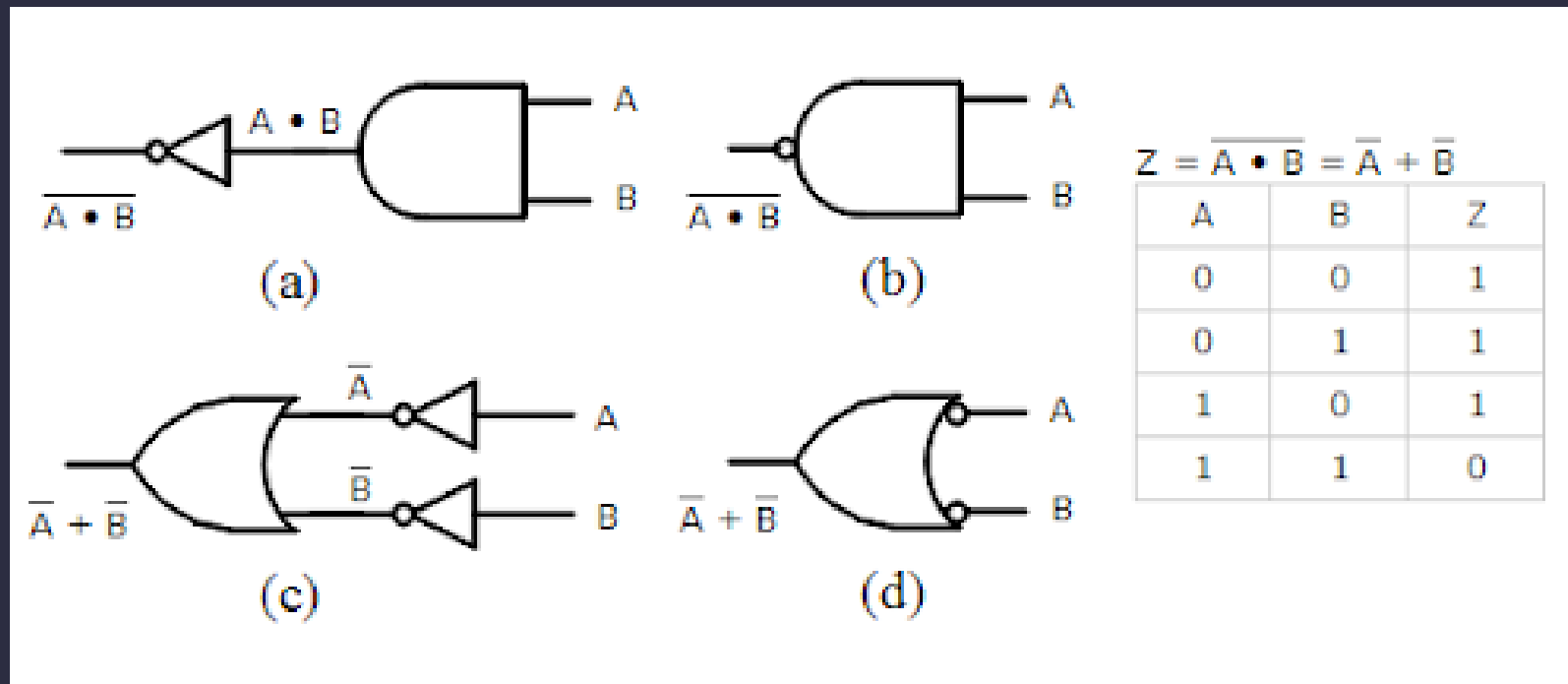


Covered Topics



Course Plan

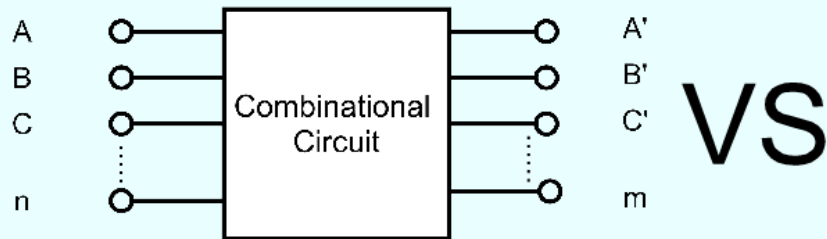
- Logic Gates & Arithmetic



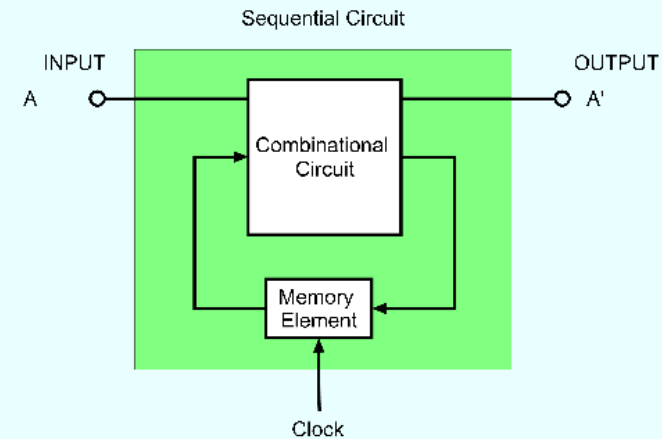
Course Plan

- Combinational and Sequential Circuits

Combinational & Sequential Circuit

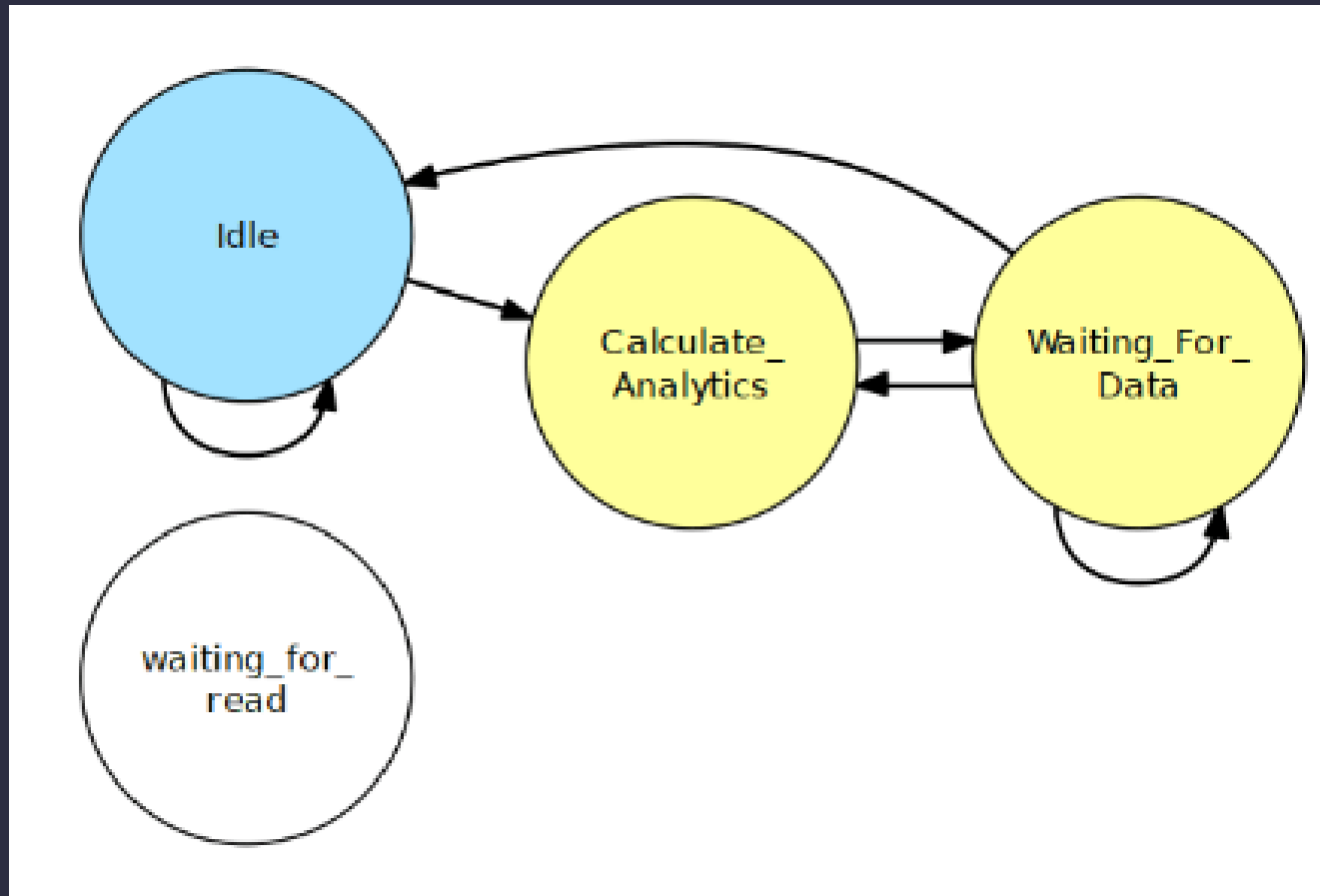


VS



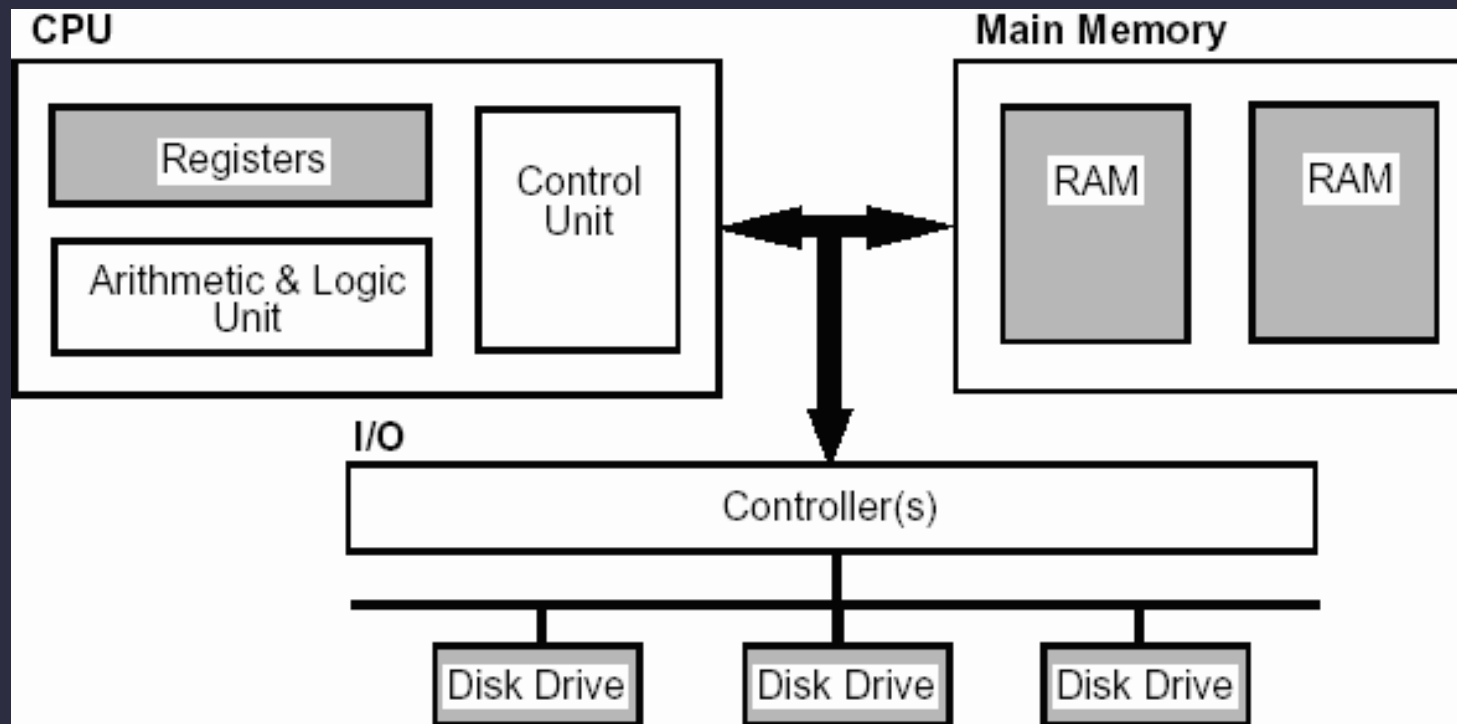
Course Plan

- Finite State Machines



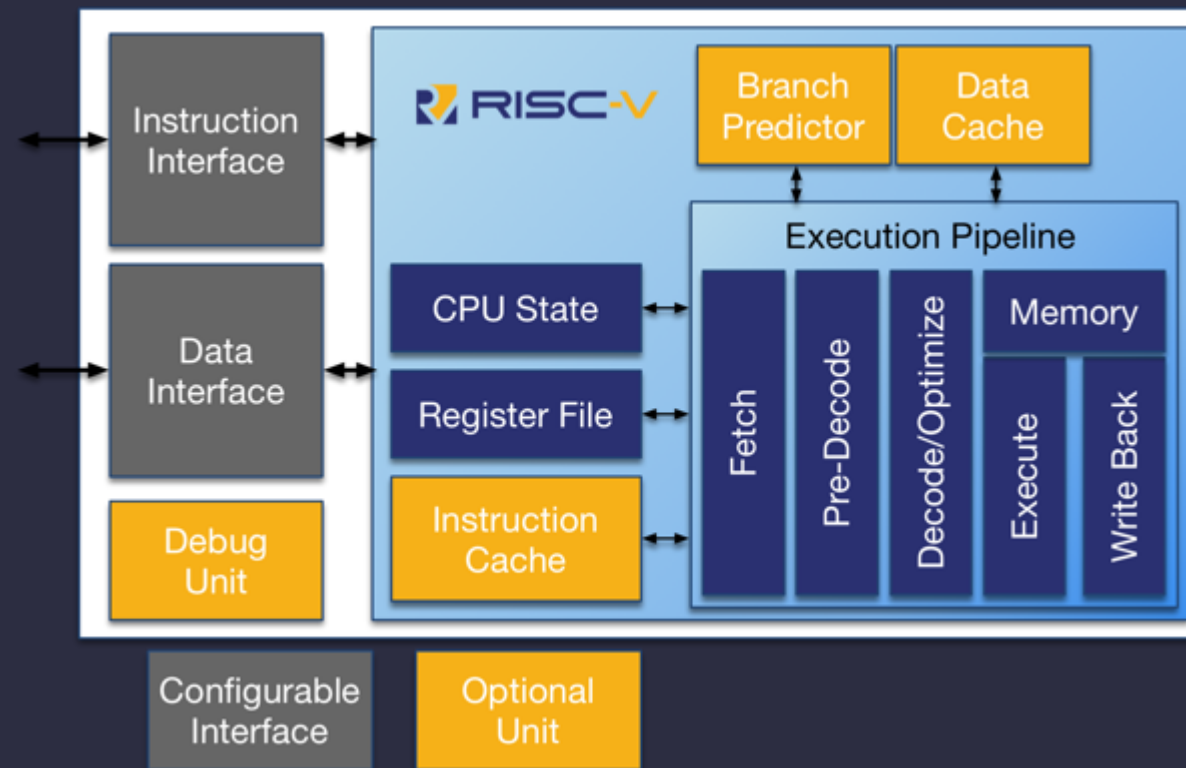
Course Plan

- Memories



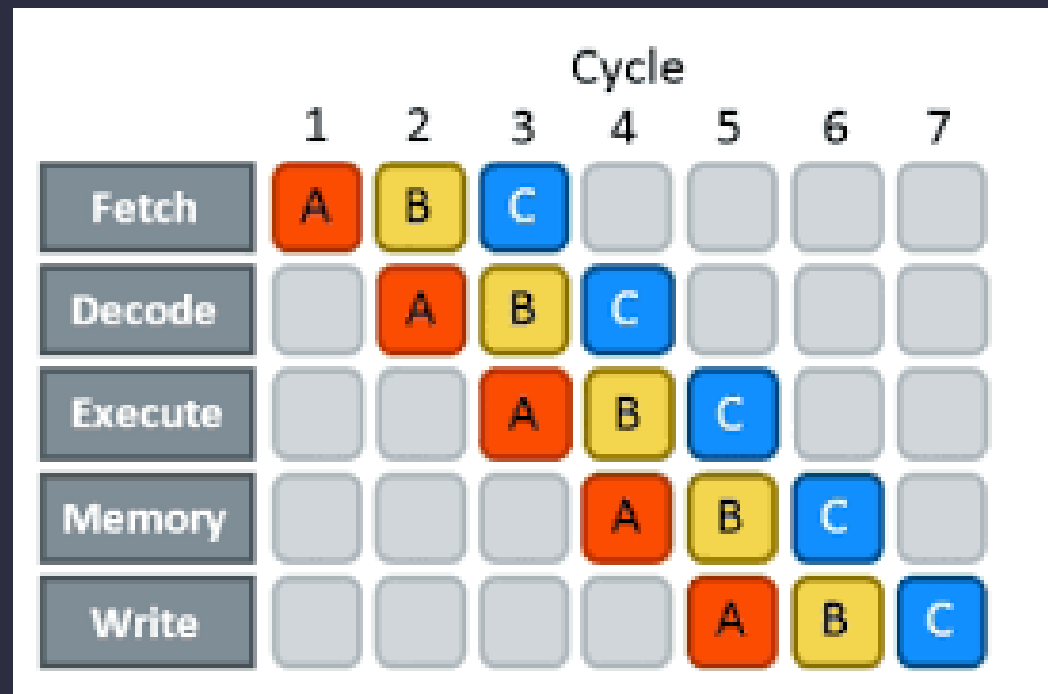
Course Plan

- RISC-V Processor



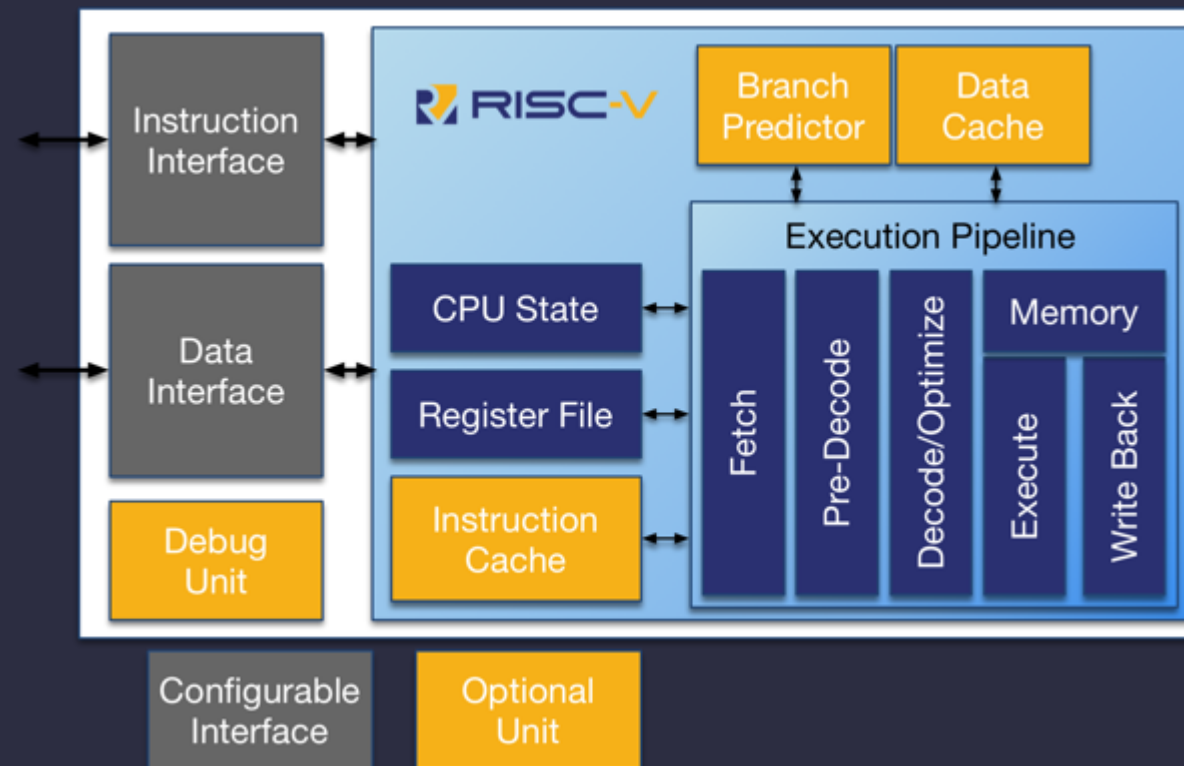
Course Plan

- Pipelining and Performance



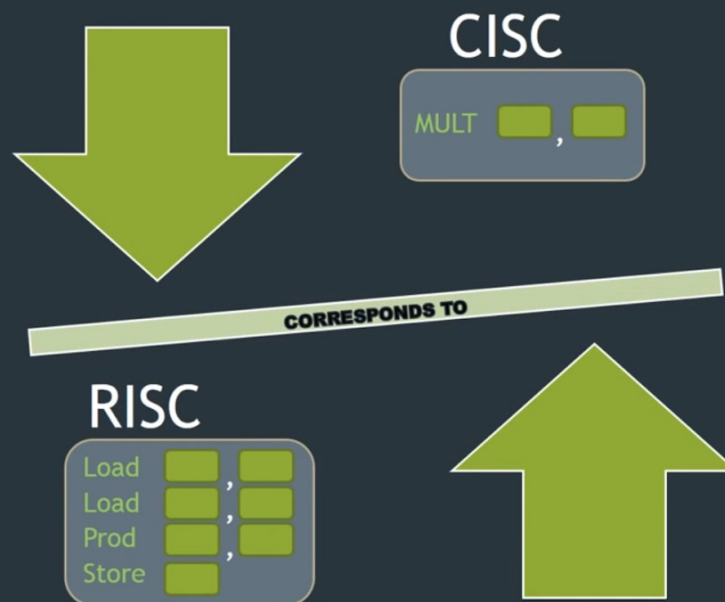
Course Plan

- RISC-V Processor Design



Course Plan

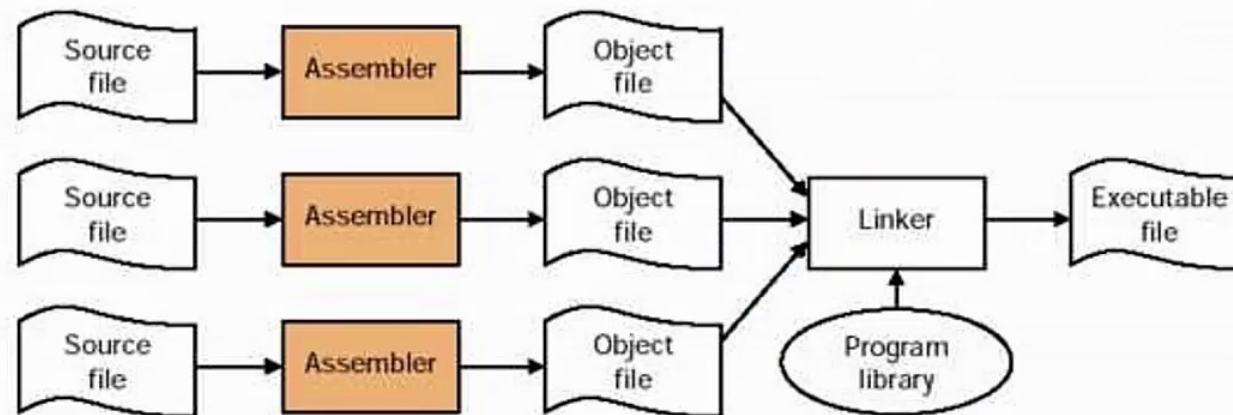
- RISC, CISC, ISA and Callings



Course Plan

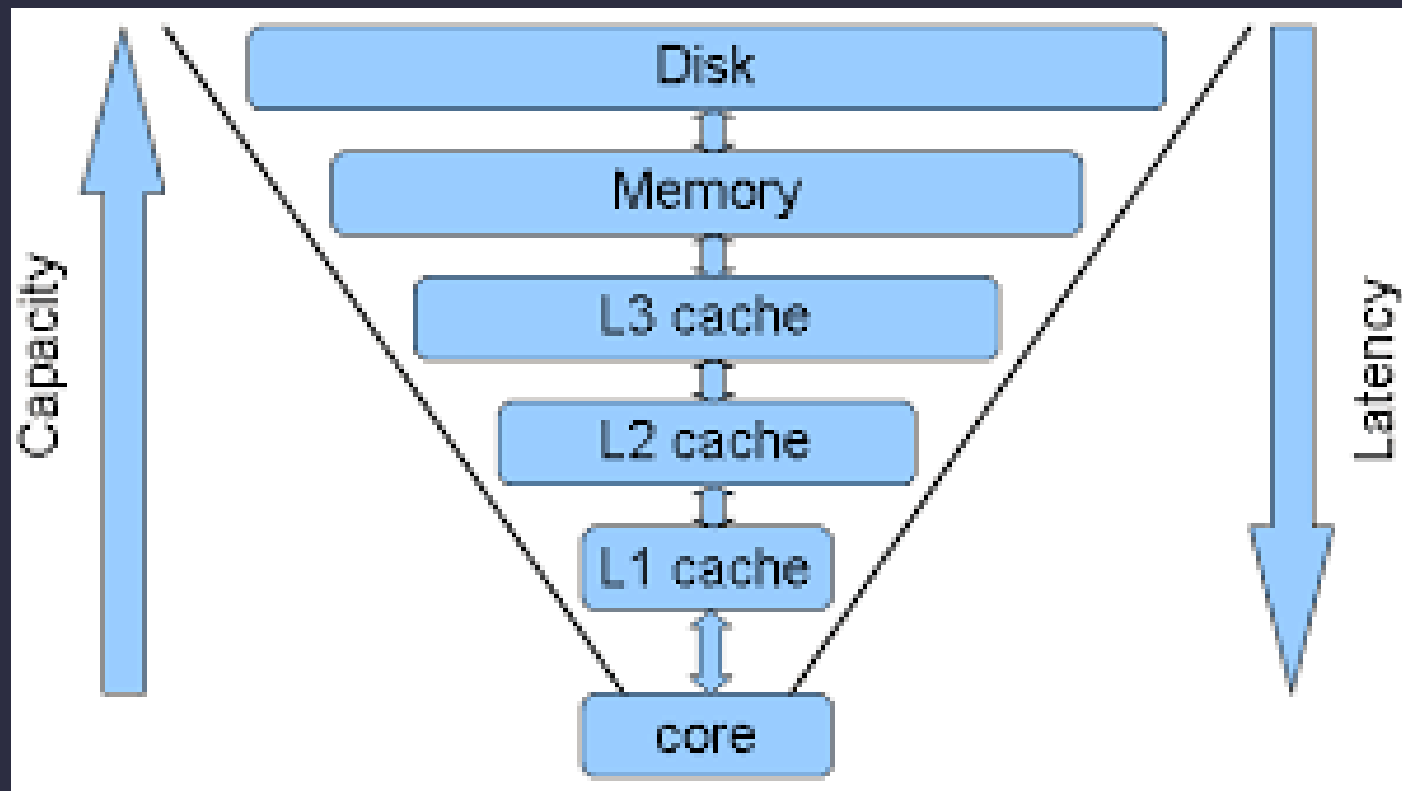
- Assembler, Linker and Loader

Compile, assemble, and link to executable
`gcc test.c` produces `test.exe`



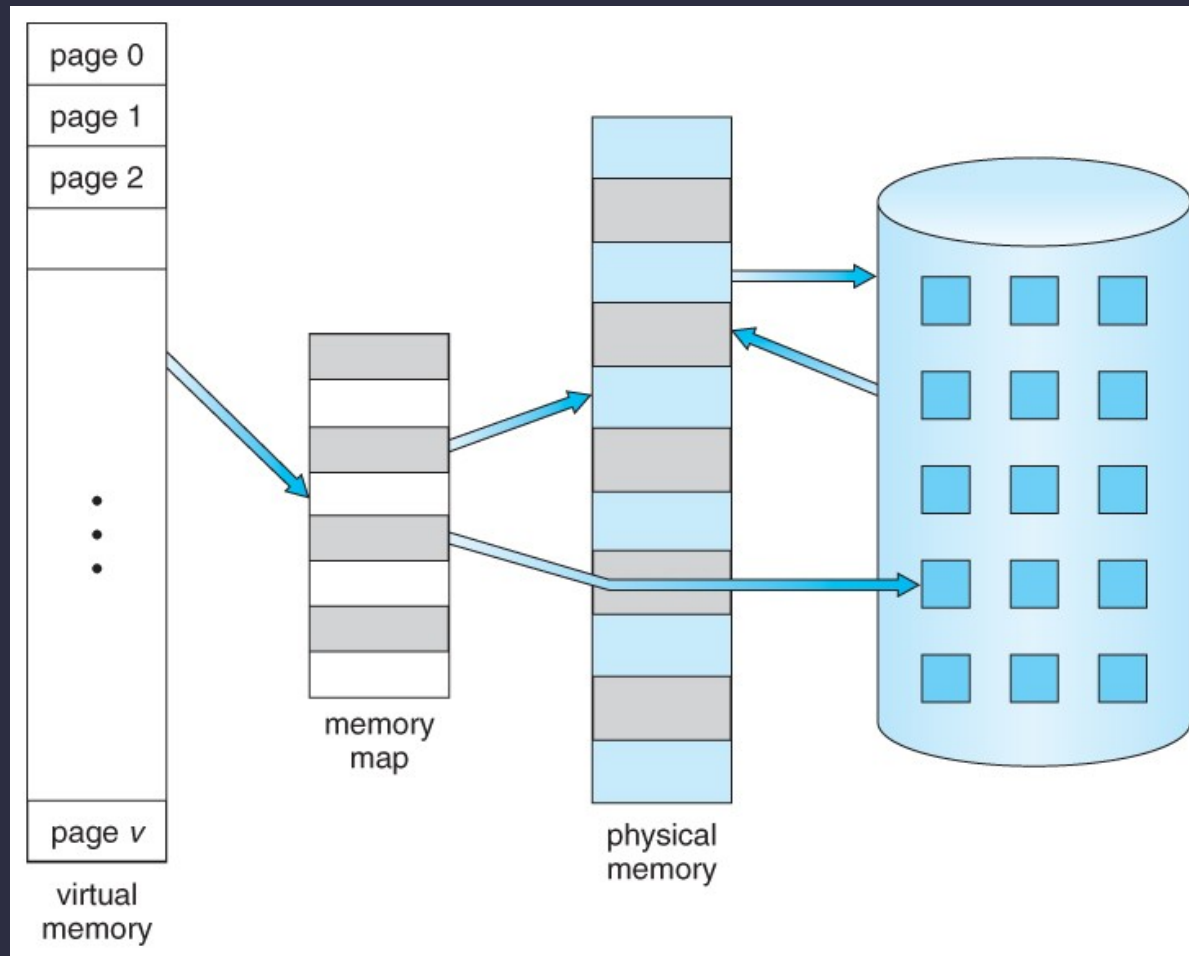
Course Plan

- Caches



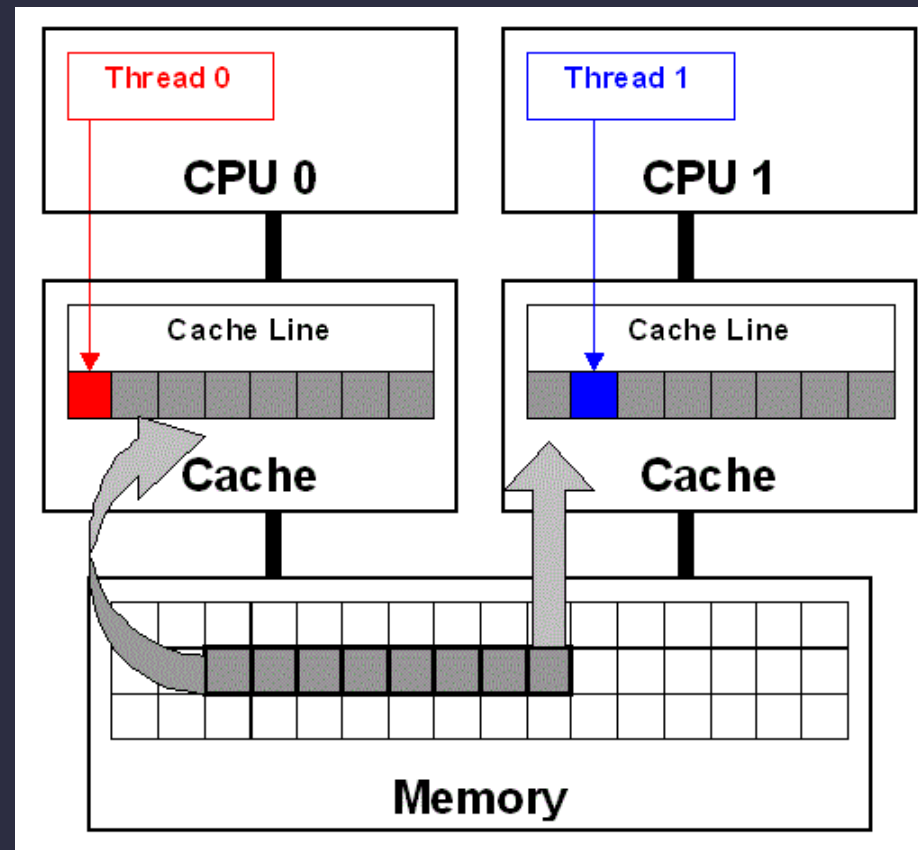
Course Plan

- Virtual Memory, System Calls and Interrupts



Course Plan

- Parallelism, Multicore and Synchronisation



Course Contents



Milli işlemci ÇAKIL, RISC-V Tabanlı

Course Contents

Website: levent.tc

Courses> BLM202 - Computer Architecture

Course Contents

Course Page Content;

- Syllabus
- Course Schedule
- Course Notes
- Homeworks
- Projects
- Exams
- LMS and Piazza
- Notes
- Feedback

Course Contents

Syllabus;

Lesson hours;

Monday 9.00-15.00

Office Hours;

Dr. Vecdi Emre Levent - Thursday 15.00-17.00

Assistant. Uğur Özbalkan - Tuesday 16.00-17.00, Friday 16.00-17.00

Course Contents

Syllabus;

Between 4-6 homework will be given.

2 Quizzes will be held.

Class attendance is compulsory at a rate of 80%.

Course Contents

Evaluation weights

Delivery time for assignments and quizzes
for every passing hour
5 points will be deducted.

Activities	Percentages
Midterm	%20
Homework / Quiz	%10
Lab	%15
Projets	%30
Final	%25
Bonus	Up to 5 points

Course Contents

Syllabus;

Grades

Point	Weight	Letter Grade
90-100	4.00	AA
85-89	3.50	BA
80-84	3.00	BB
75-79	2.50	CB
65-74	2.00	CC
50-64	1.50	DC
45-49	1.00	DD
0 -44	0	FF

Course Contents

Syllabus;

Expected effort

190 hours in total
effort is expected.

Counnt	Hour	#Times	Total
Preparation	2	14	28
Repetition	2	14	28
Homeworks	4	6	24
Project	48	1	48
Course	4	14	56
Midterm and Finals	3	2	6

Course Contents

Academic honesty



Cheat

Working together

Course Contents

Course schedule

Week	Topic
1	Introduction
2	Logic Gates and Arithmetic
3	Combinational and Sequential Circuits
4	Finite State Machines
5	Memories
6	RISC-V Processor
7	Pipelining and Performance
8	Midterm
9	RISC-V Processor Design
10	RISC, CISC ISA and Calls
11	Assemblers, Linkers and Loaders
12	Cache's
13	Virtual Memory, System Calls and Interrupts
14	Parallelism, Multi-Core and Synchronization
15	Final

Course Contents

Homeworks;

The assignments to be given and their solutions will be shared on the homework page.

Course Contents

Projects;

Projects to be completed by each student will be announced at the end of the term.

Course Contents

Exams;

Sample questions and solutions of exams will be shared for midterm and final exams.

Course Contents

LMS and Piazza;

The LMS system is the system where we will request some assignments to be uploaded. The system will automatically closed on the last upload date.

The Piazza system is a classroom question and answer platform. Whenever you have a topic about lecture, homework or exams, you can write on this platform. The questions you write are seen by teachers and students. You can also help each other measuredly through this platform.

Course Contents

Grades;

On the Grades page, all the grades you have collected in the course are given.

You can see how many points you have collected from midterm, homework, quiz, lab, final and bonuses by browsing through the pages.

Course Contents

Feedback,

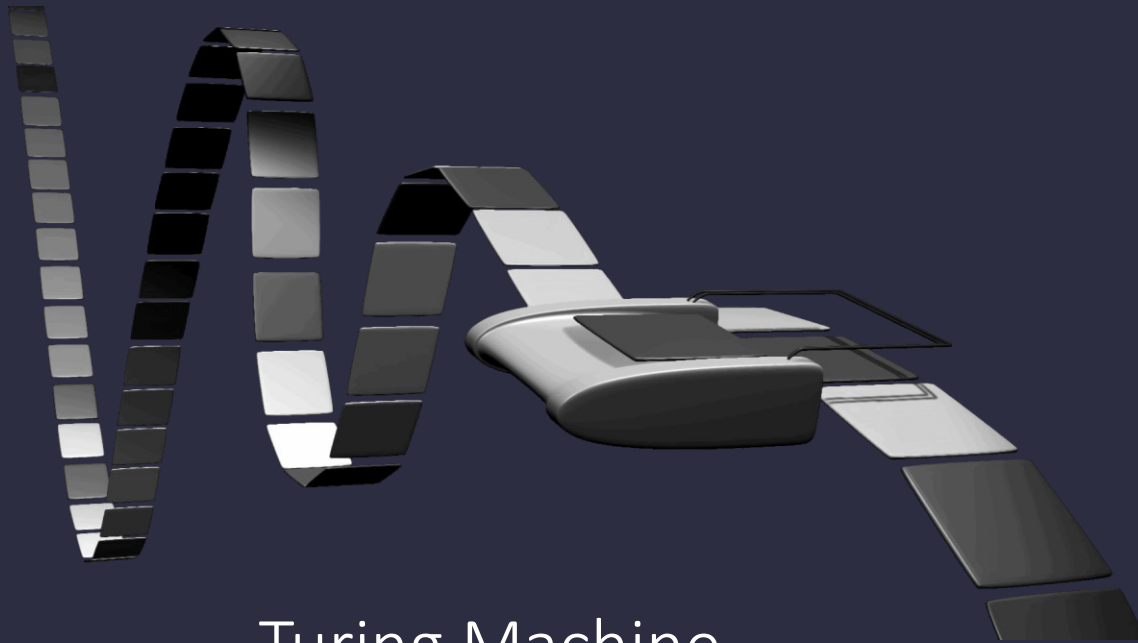
Feedback is very important for improving the quality of the lesson.

You can comment on the feedback mechanism that will be created every week through the LMS system.

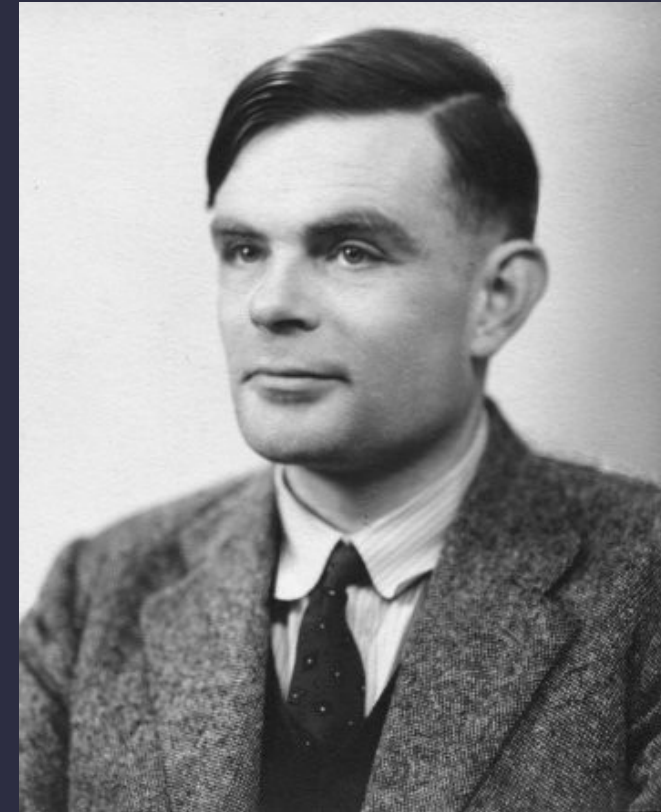
Each time you make a comment, an additional 0.5 bonus points will be given to your end of year score.

You can collect a maximum of 5 points bonus.

Computer Architecture



Turing Machine
1936



Alan Turing

Computer Architecture



Enigma Machine

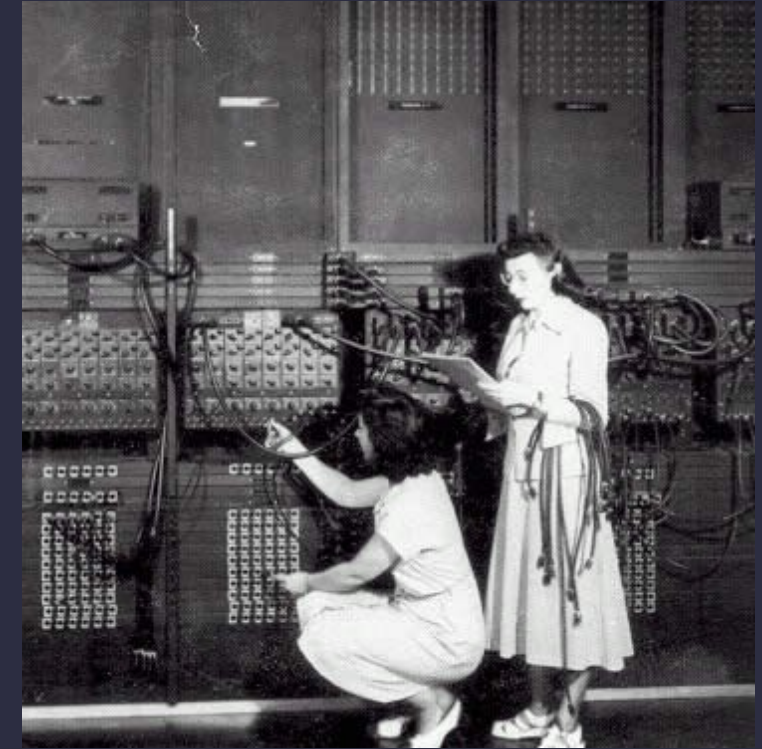
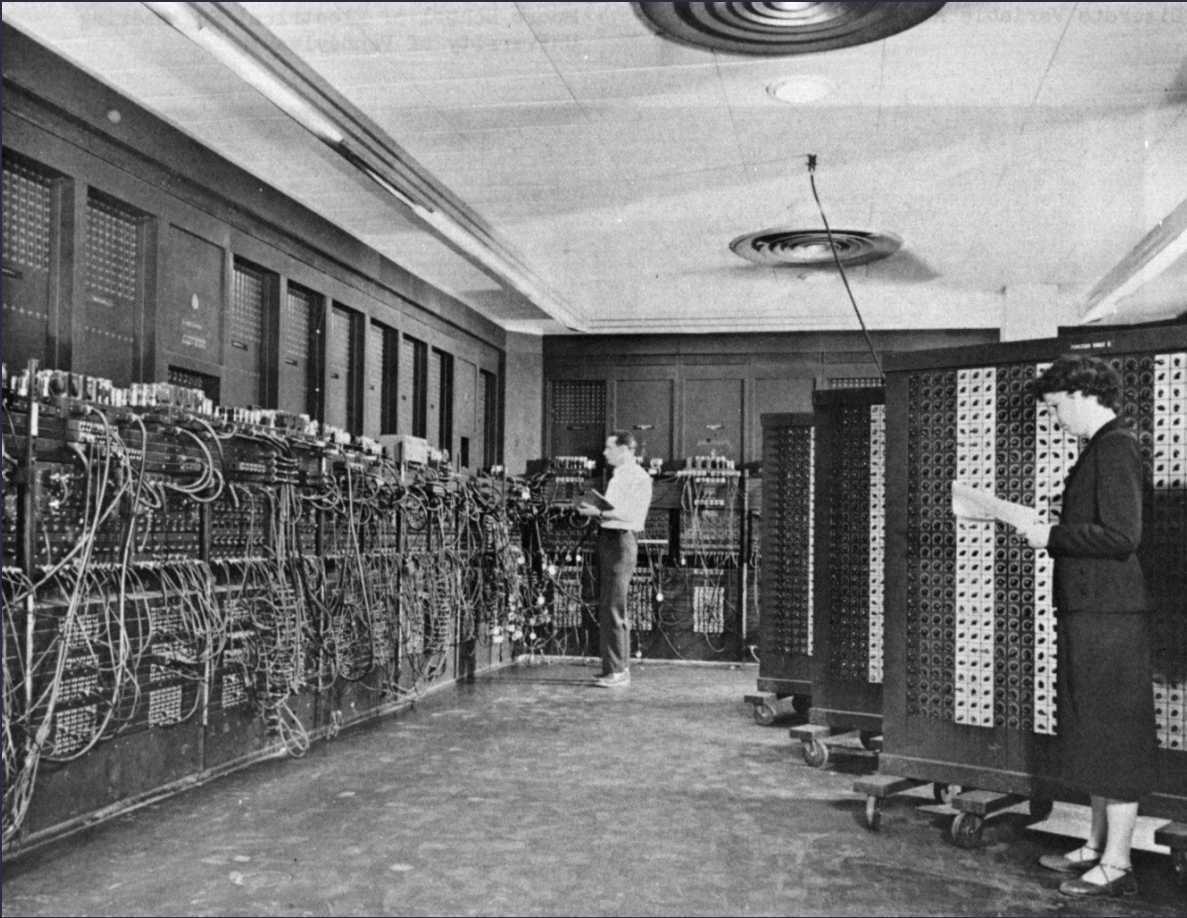
At the world war II, used by germans for encrypted communication



The Bombe

It designed for decrypting encrypted messages by Enigma machine. Designed by Alan Turing.

ENIAC (Electronic Numerical Integrator And Computer)



1946
John Mauchly
J. Presper Eckert

IBM 7090 Human Computers programming the IBM 7090



1959

Course Objectives

- Hardware / Software Interaction
 - How CPU works?
 - How computer architecture designed?
- Fundamentals of developing applications
 - Quality
 - Quality = Correct, fast, safe
 - Understanding the current technology

Course Objectives

```
#include <stdio.h>

int main() {
    printf("Hello world!\n");
    return 0;
}
```

You will learn, how this code
executing by CPU at the end of
lecture

Compiler and Assemblers

C

```
int x = 10;
x = 2 * x + 15;
```

compiler

r0 = 0

RISC-V
Assembly
Language

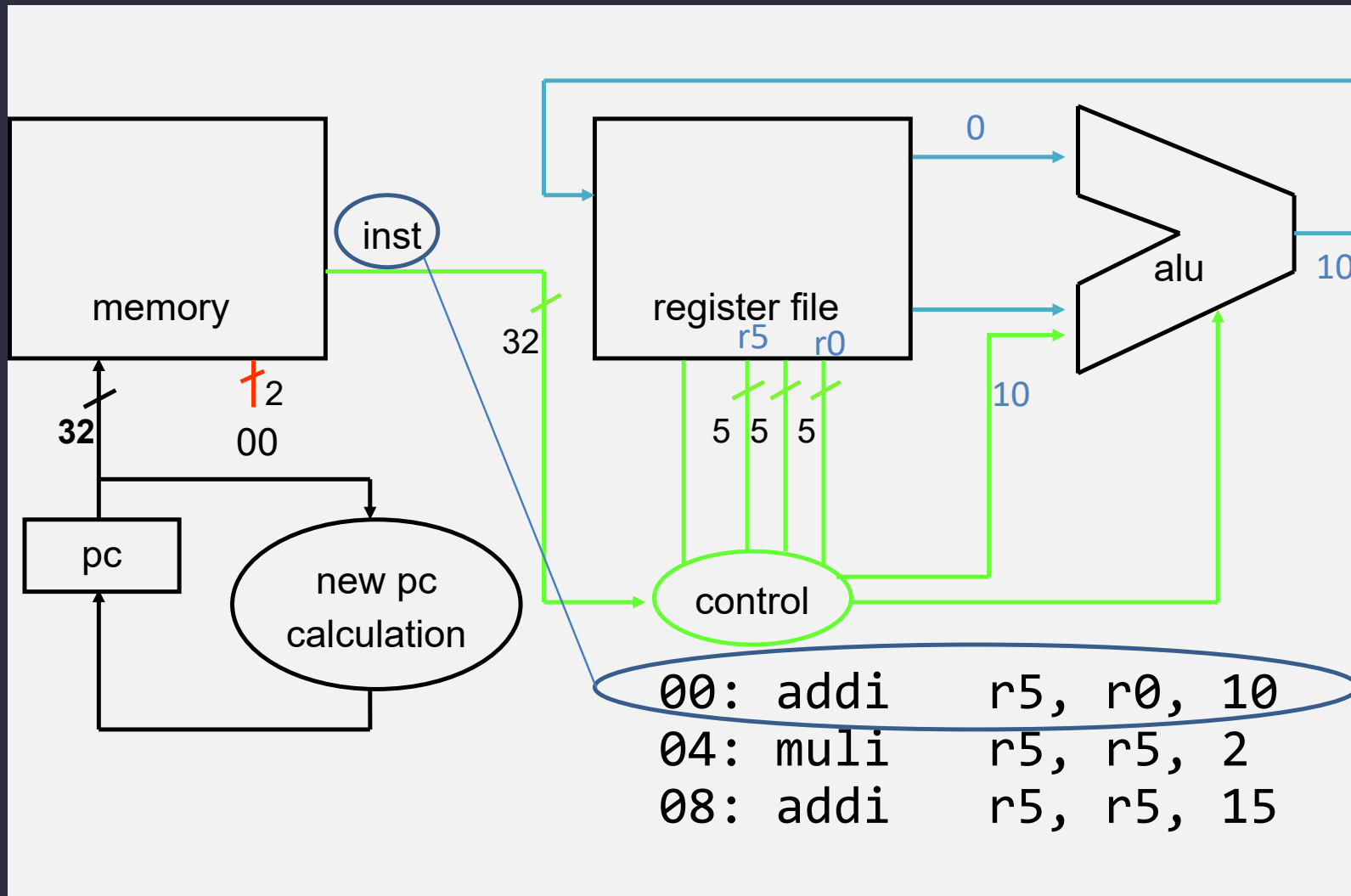
```
addi r5, r0, 10 ← r5 = r0 + 10
mulr r5, r5, 2 ← r5 = r5 * 2
addi r5, r5, 15 ← r5 = r5 + 15
```

assembler

RISC-V
Makina
Language

10	r0	r5	op = addi
000000001010000000001010010011			
000000000000100101001001010011			
00000000111100101000001010010011			
15	r5	r5	op = addi

Simple CPU Design



Instruction Set Architecture (ISA)

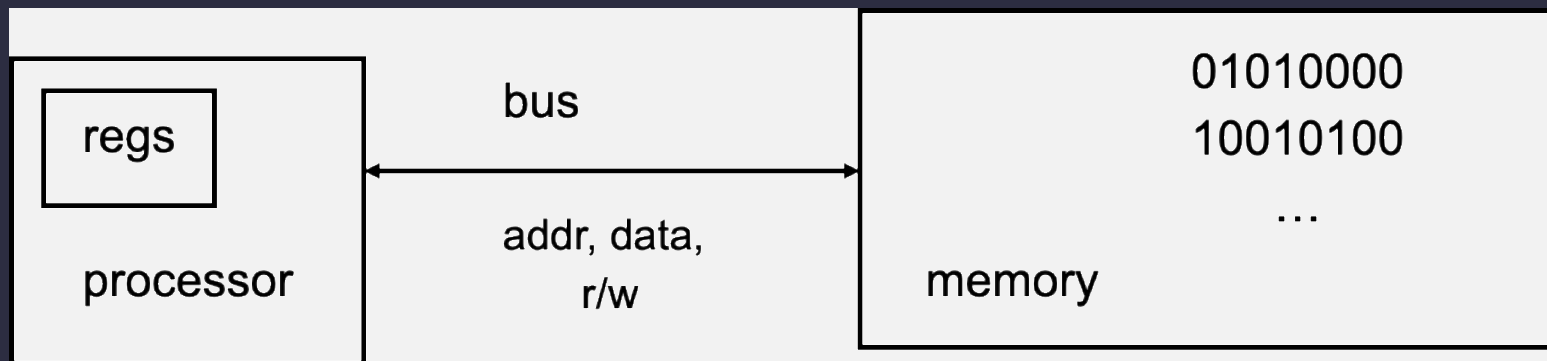
Instruction Set Architecture (ISA),

It is the relationship between hardware and software.

It specifies the supported operations of CPU and defines how they can be used

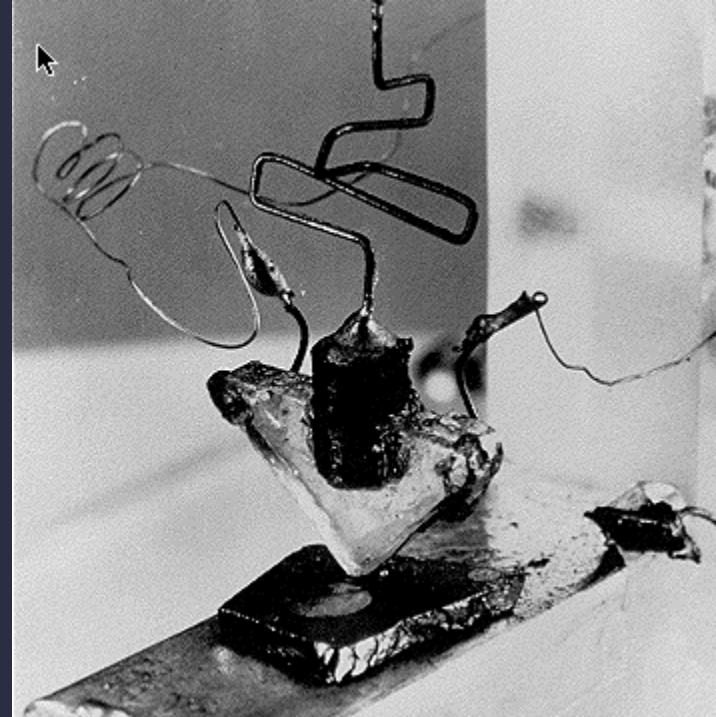
Simple Computer System

- A CPU executes instructions
 - CPUs stores some executions in the internal registers
- In the memory, instructions and datas stored
 - In the Von Neumann architecture, instructions and datas are stored at the same memory.



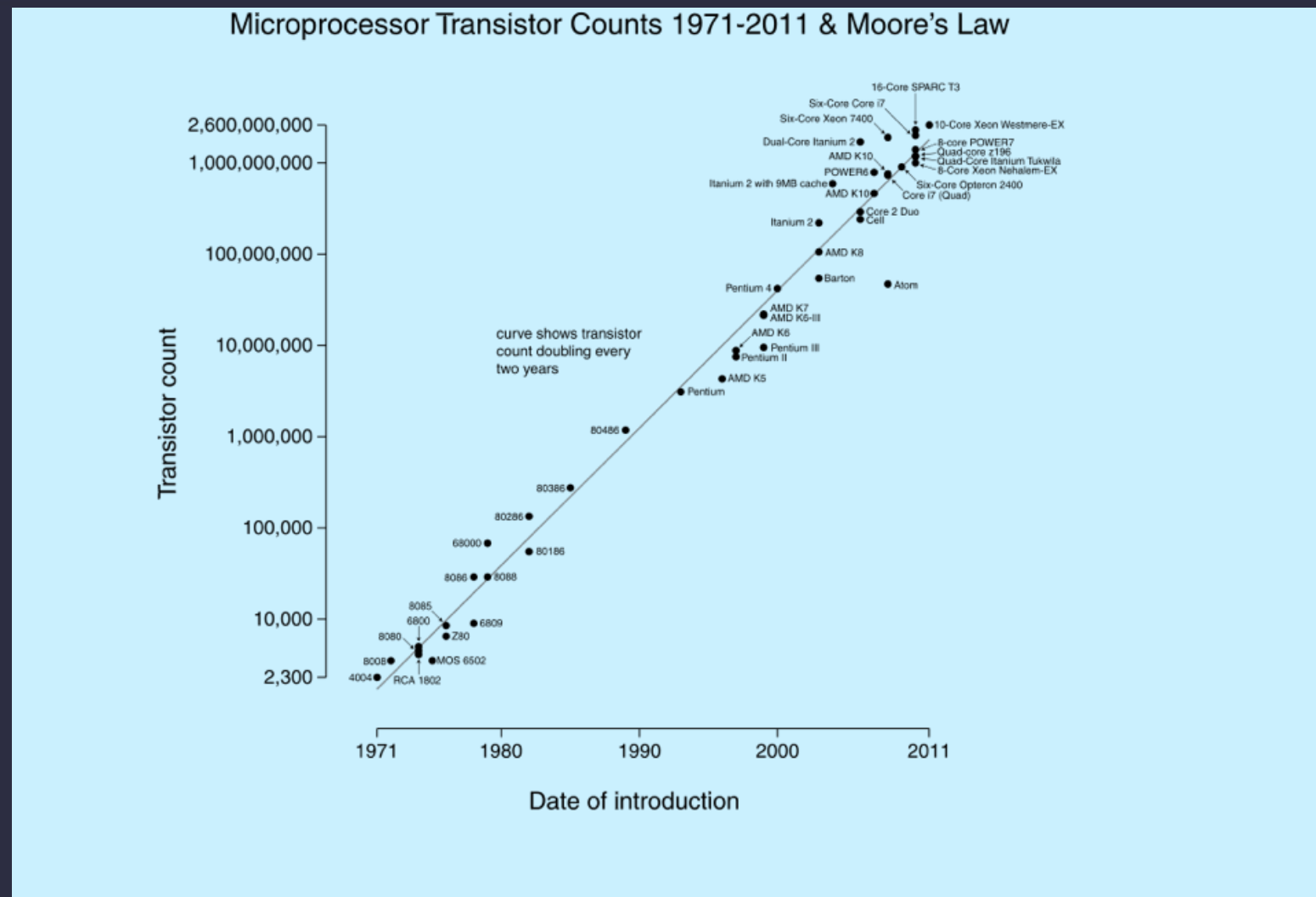
When started?

- Electric switches
 - On/Off
 - Binary
- Transistor

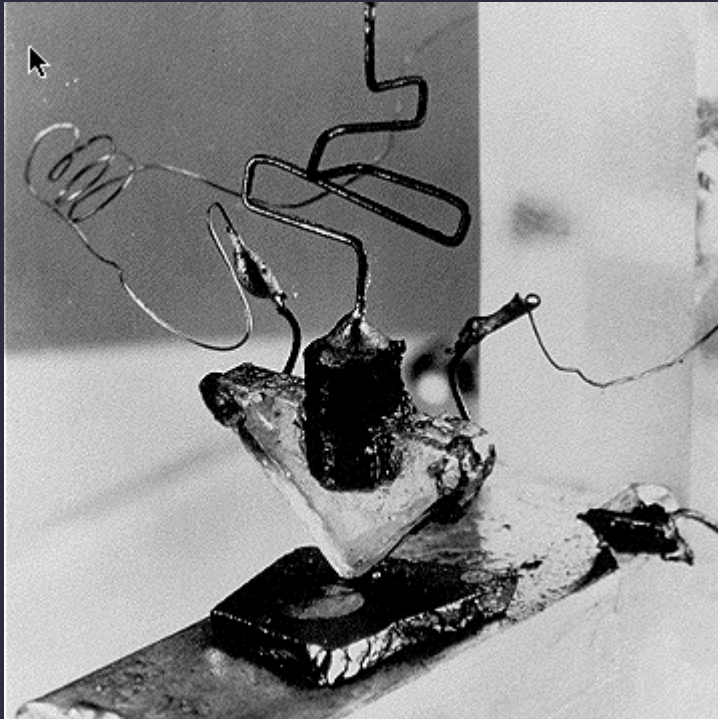


First transistor at Bell Labs

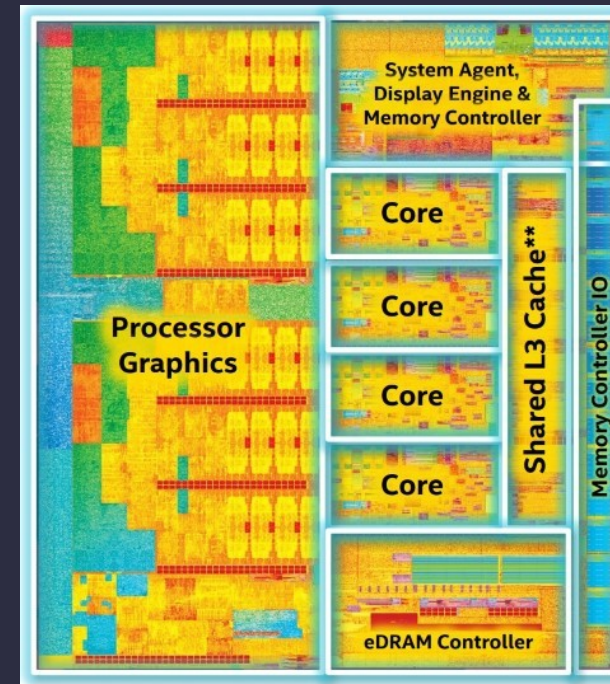
Moore's Law



Before and After



- First Transistor
 - AT&T Bell Labs
 - 1947



- Intel Broadwell CPU
 - 7.2 billion transistor, 14nm
 - 22 cores