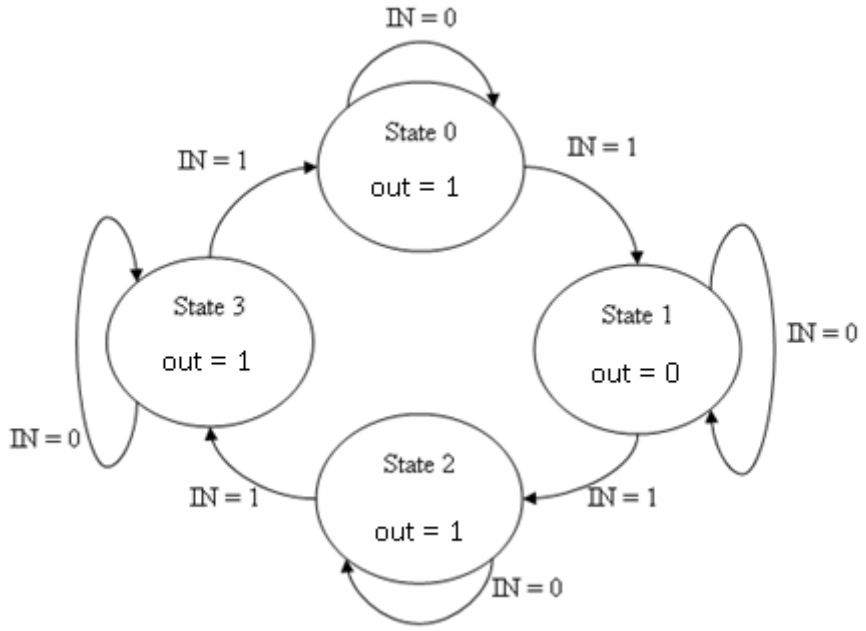
Fenerbahçe University

BLM 201 – Digital Design

State Machines

Question:

Implement design and simulate with verilog language of given state machine.



Note 1: Please contact the course's piazza page if you have any questions.

Note 2: The homework can be handwritten or computer-printed (You will upload it to Blackboard).

Note 3: Your name, surname, school number and number of homework should be included in your homework paper.

Note 4: Please follow the rules of academic honesty (There are rules on the course page).