Fenerbahce University

BLM 201 – Logical System Design

LAB 1: Combinational Circuits

About LAB:

Introduction to Verilog Language, designing combinational circuits

Stages and scores of LAB :

1- Preliminary stage (0 Points)

In the Vivado design tool, Open an empty project for the XC7A35Tcpg236-1 (Basys 3) device.

Download the constraint file prepared for Basys3.

http://levent.tc/files/courses/digital_design/labs/basys3.xdc

A module called testModule will be developed. The input and output signals of the module are given as follows.

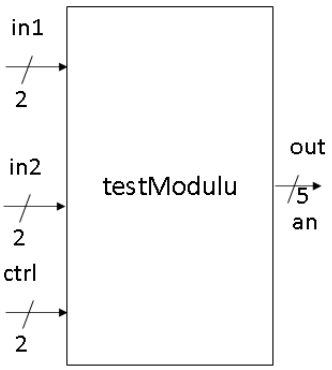

Figure 1. Test Module Inputs Outputs

This module produces output from the out port by performing arithmetic operations with in1 and in2 according to the value of the ctrl input.

- if ctrl == 0, out = in1 + in2
- If ctrl == 1, out = in1 – in2
- If ctrl == 2, out = in1 * in2
- Else, out = 5'b11111

Solution:

```
` timescale 1ns / 1ps

module testModule (input [1:0] in1, input [1:0] in2, input [1:0] ctrl, output reg [4:0] out
);

   always @(*) begin
      if ( ctrl ==0)
         out = in1 + in2;
      else if ( ctrl ==1)
         out = in1 - in2;
      else if ( ctrl == 2)
         out = in1 * in2;
      else
         out = 5'b11111;
   end

endmodule
```

Use switches and LED for test this design at FPGA.

2- Design the below circuit with verilog language

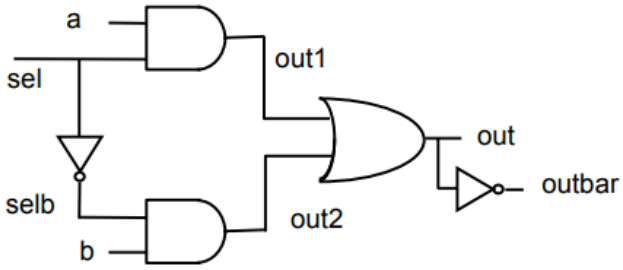

Figure 4. Reference Design

3- Design a decoder with 3 bits of input and outputs 8 bits of output.

Example 2-bit decoder :

```
` timescale 1ns / 1ps

module testModulu ( input [1:0] in , output reg [2:0] out );

   always @(*) begin
      if (in ==0)
         out = 4'b0001;
      else if (in == 1)
         out = 4'b0010;
      else if (in == 2)
         out = 4'b0100;
      else if (in == 3)
         out = 4'b1000;
   end

endmodule
```