Fenerbahçe University

BLM 201 – Digital Design

LAB 3: Verification

Important Note: As you complete the stages, call the instructor or assistant of the course and show the stage you have completed, and then move on to the next stage.

About LAB: Verification with Verilog

LAB stages:

1- Preliminary stages (0 Point)

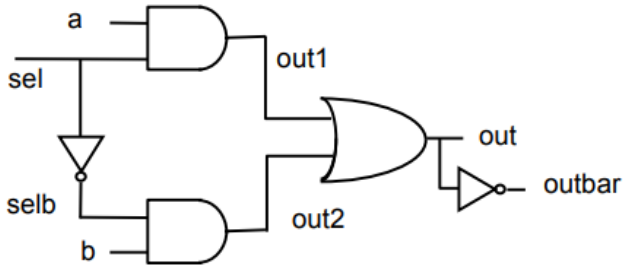
Create a Vivado Project with XC7A35Tcpg236-1 (Basys 3) device.

Prepare a testbench module for the module named testModule, whose RTL design is given below, and test it. During the test process, change the inputs every 5 ns, feed the inputs to test the addition, subtraction and multiplication of the design and observe the results.

```
`timescale 1ns / 1ps

module testModule(input [1:0] in1, input [1:0] in2, input [1:0] ctrl, output reg [4:0]
out);

   always@(*) begin
      if(ctrl==0)
         out = in1 + in2;
      else if(ctrl==1)
         out = in1 - in2;
      else if(ctrl == 2)
         out = in1 * in2;
      else
         out = 5'b11111;
   end

endmodule
```

1- Combinational Circuit (50 Point)

Write the verilog design of the combinational circuit given below. Verify the design with designing a testbench.



2- Knight Rider Simulation (50 Point)

A module named KnightRider will be designed. This module takes a one-bit input called clk, rst and produces output called 8-bit LED.

The task of the module is to show the number 8'b10000000 when rst is pressed, then move to the far right, and move to the left when it reaches the far right. This cycle will repeat endlessly.

Example pattern is given below. Design will be for 8-bit LEDs.

X 0 0 0

0 X 0 0

0 0 X 0

0 0 0 X

0 0 X 0

0 X 0 0

X 0 0 0

0 X 0 0

…

Develop a Verilog design of the module whose behavior is specified. Verify the designed module in the simulation environment.