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| **Fenerbahçe University** |
| **COMP 2001 – Logical System Design**  **Lab Document** |
| **LAB …: …** |

**Student No: …**

**Name: …**

**Surname: …**

**Solutions**

**Not**: Solutions may consist of RTL (Verilog), schematic representation, simulation screenshots. Depending on the lab question, you can use one or more of these approaches.

**Solution 1:**

**Solution 2:**

**Solution 3:**