Mantıksal Sistem Tasarımı – BLM 201

Hafta 3: Kombinasyonel Lojik
Bölüm IV

Fenerbahçe Üniversitesi

3. Hafta İçeriği

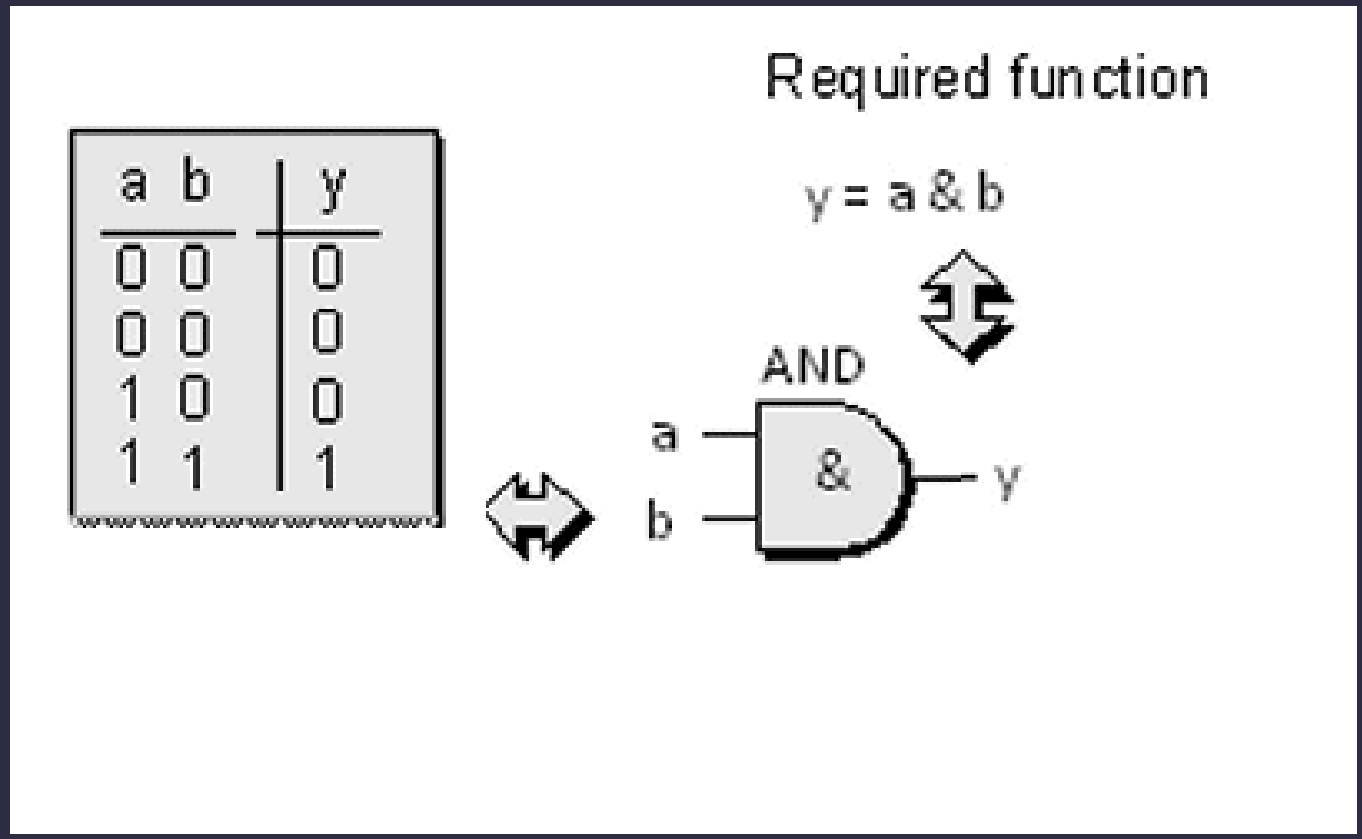
- Kombinasyonel Devreler (Combinational Circuits)
  - Verilog'a Giriş

Verilog – Kombinasyonel Devreler

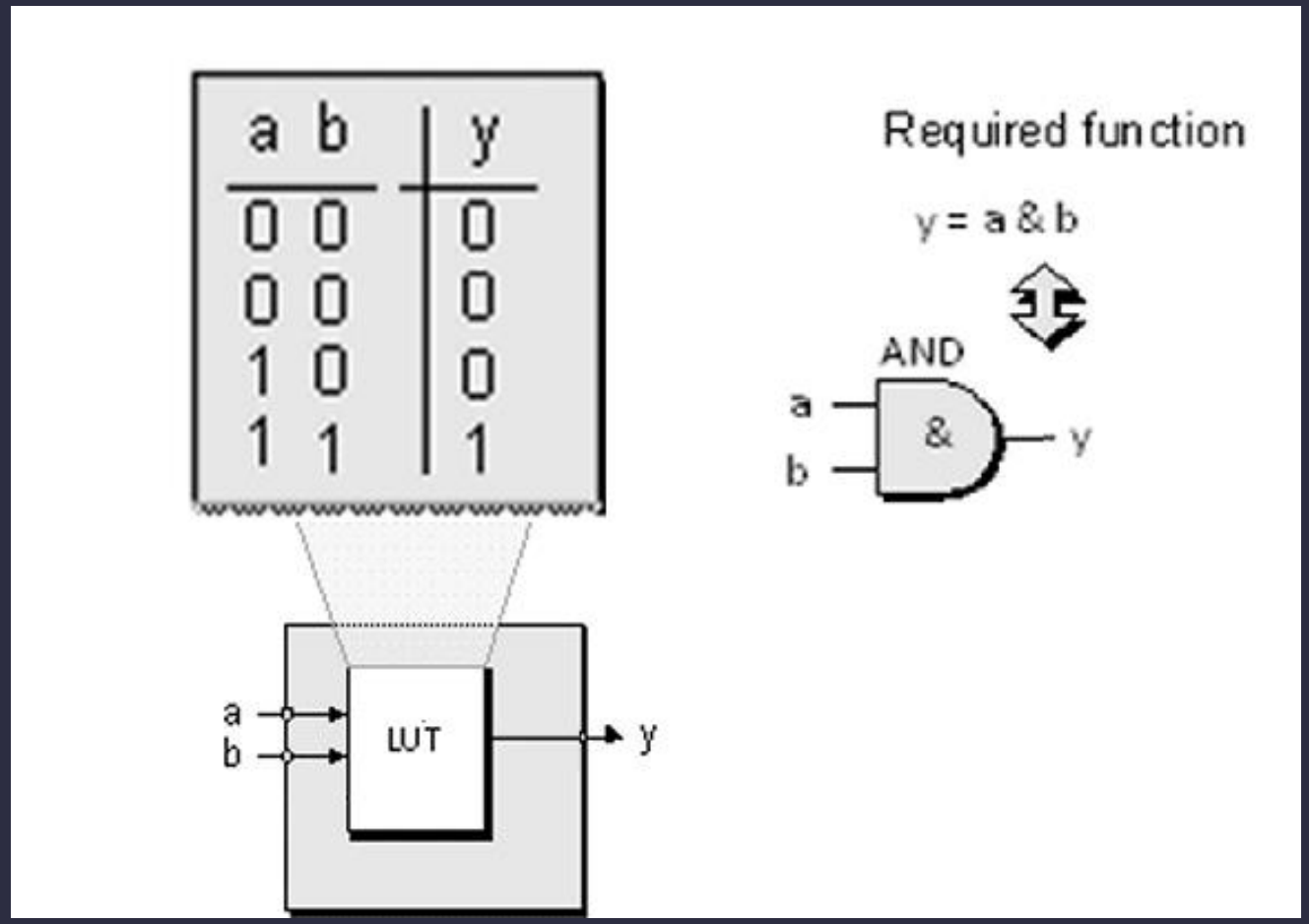
Öne çıkan HDL (Hardware Description Language) Dilleri

- *Verilog*
- *System Verilog*
- *VHDL*

Verilog – Kombinasyonel Devreler



Verilog – Kombinasyonel Devreler



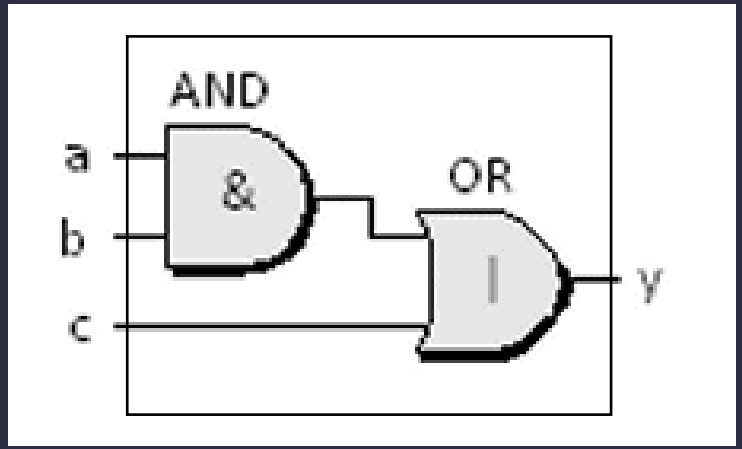
Verilog – Kombinasyonel Devreler

Vivado,

- Verilog
- System Verilog
- VHDL

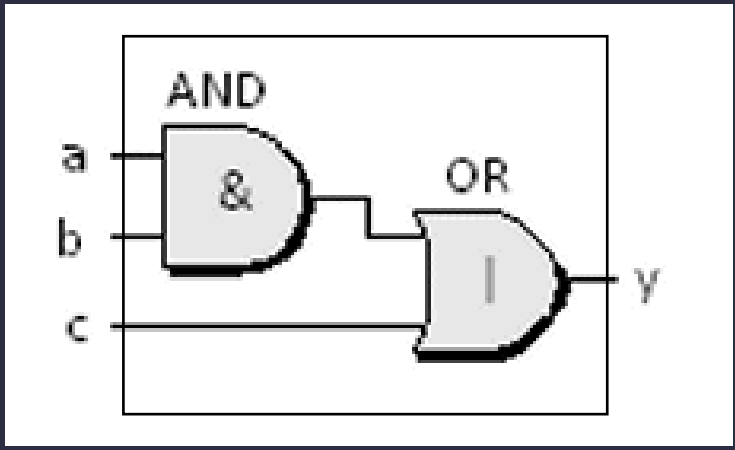
Dillerini desteklemektedir. Ders kapsamında Verilog dili ile tasarımlar yapılacaktır.

Verilog – Kombinasyonel Devreler



myModule

Verilog – Kombinasyonel Devreler



myModule

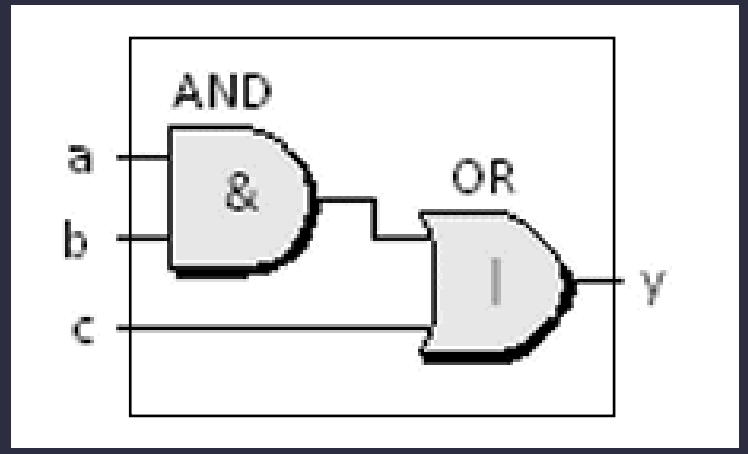
Verilog Tasarım

```
module myModule(input  a, input b, output y);



endmodule
```

Verilog – Kombinasyonel Devreler



myModule

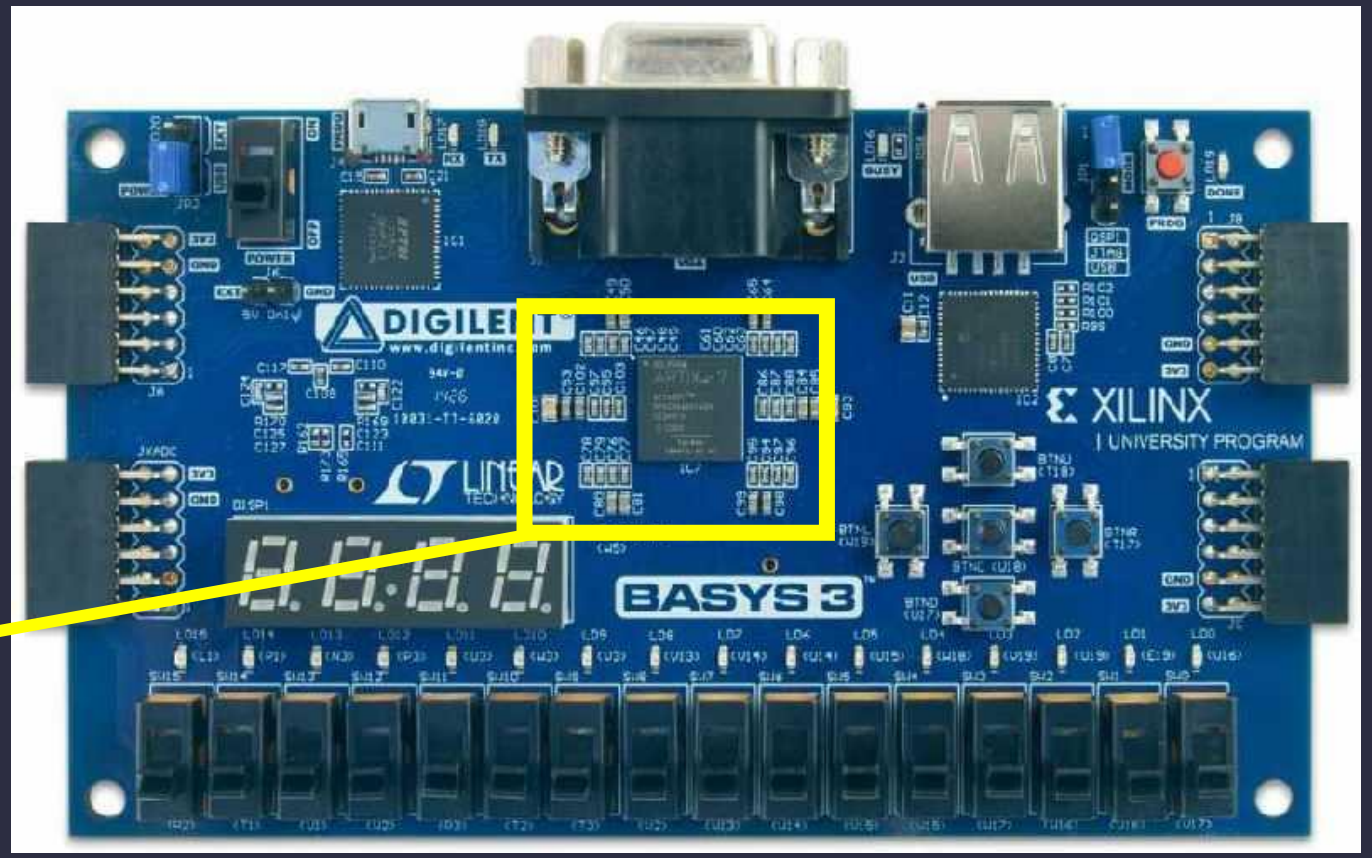
Verilog Tasarım

```
module myModule(input  a, input b, output y);

        reg tmp;
        always@(*) begin
                tmp = a & b;
                y = tmp | c;
        end

endmodule
```

Verilog – Kombinasyonel Devreler



Verilog – Kombinasyonel Devreler

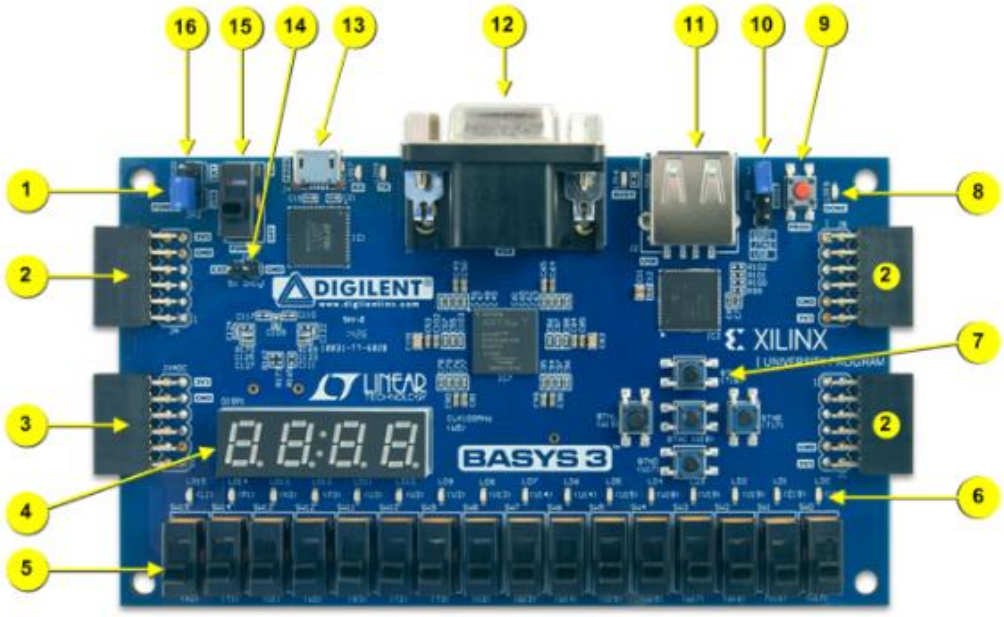
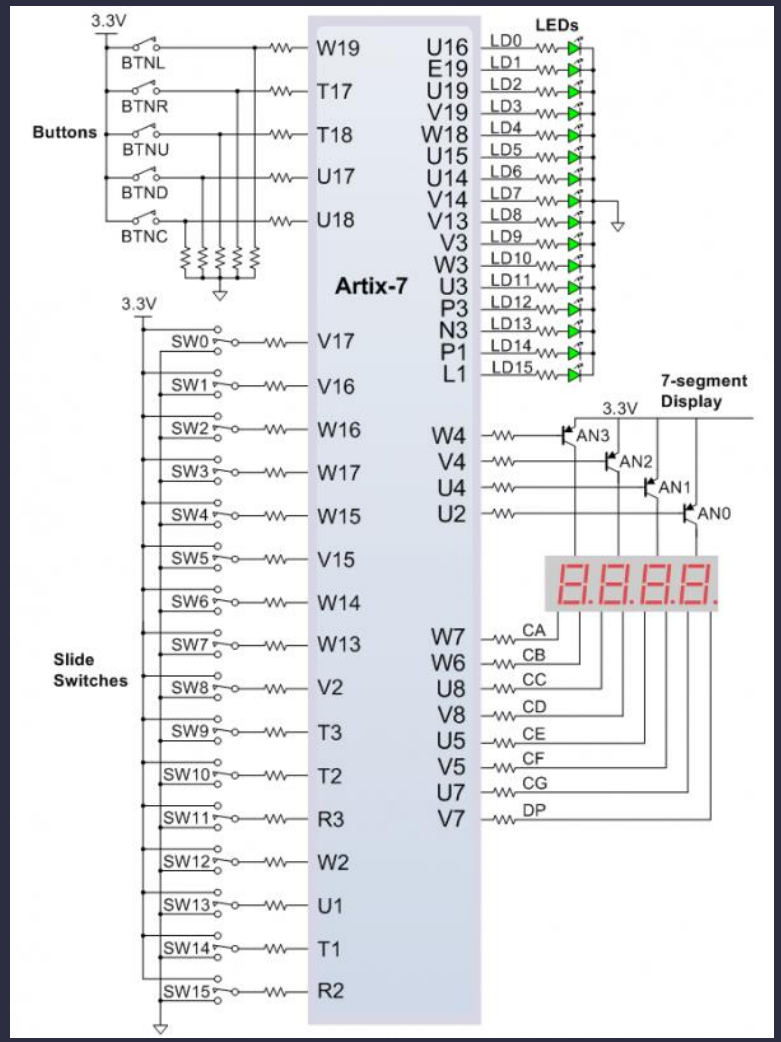


Figure 1. Basys3 board features

Callout	Component Description	Callout	Component Description
1	Power good LED	9	FPGA configuration reset button
2	Pmod connector(s)	10	Programming mode jumper
3	Analog signal Pmod connector (XADC)	11	USB host connector
4	Four digit 7-segment display	12	VGA connector
5	Slide switches (16)	13	Shared UART/ JTAG USB port
6	LEDs (16)	14	External power connector
7	Pushbuttons (5)	15	Power Switch
8	FPGA programming done LED	16	Power Select Jumper

Verilog – Kombinasyonel Devreler



Verilog – Kombinasyonel Devreler

Kısıt (XDC) Dosyası

http://levent.tc/files/courses/digital_design/labs/basys3.xdc