Digital Design

Week 3: Combinational Logic
Part III

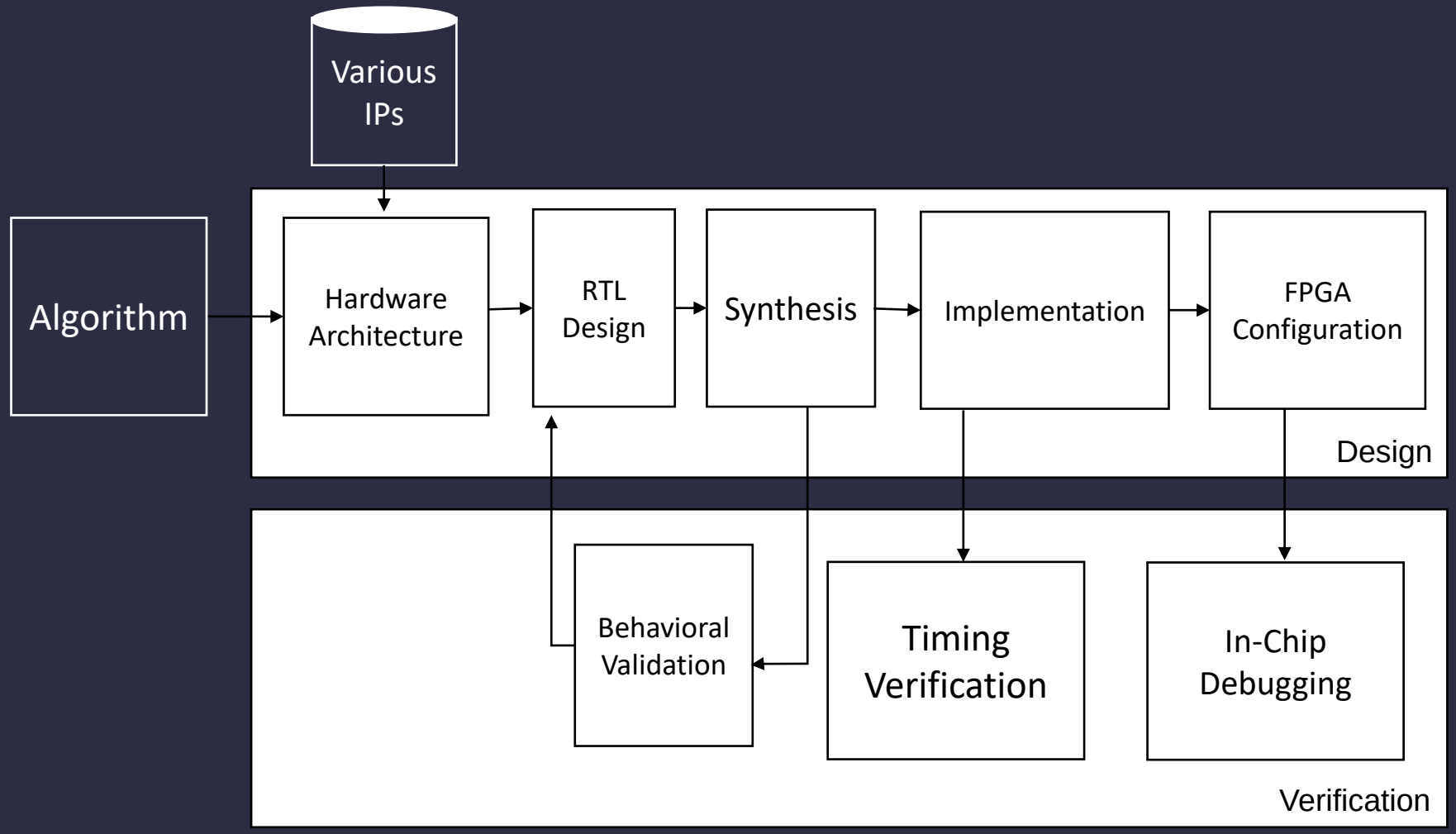
Fenerbahce University

Combinational Circuits

- Combinational Circuits
  - What is FPGA?
  - Vivado Design Tool

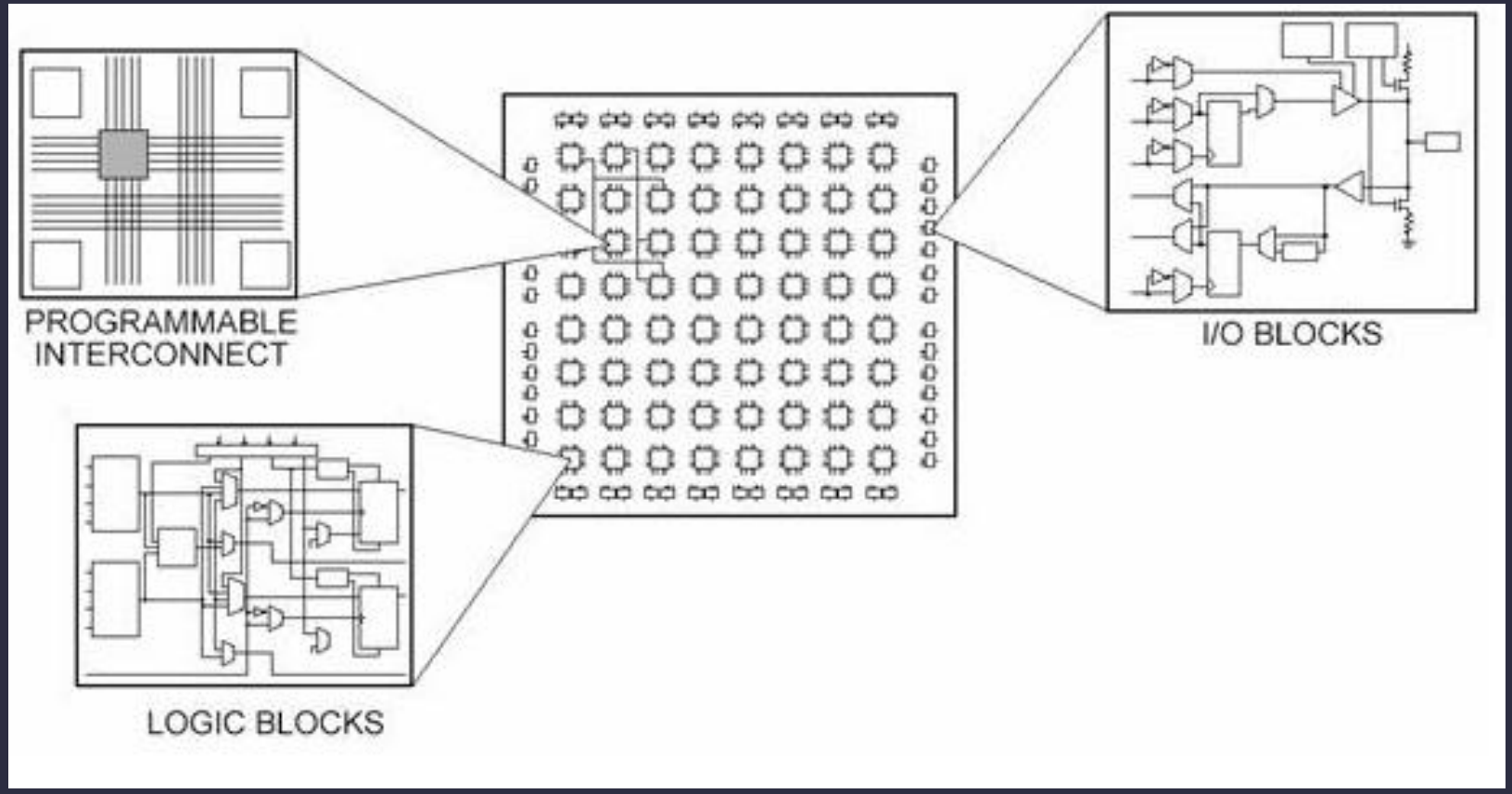
Vivado Design Tool

- *Design Flow*



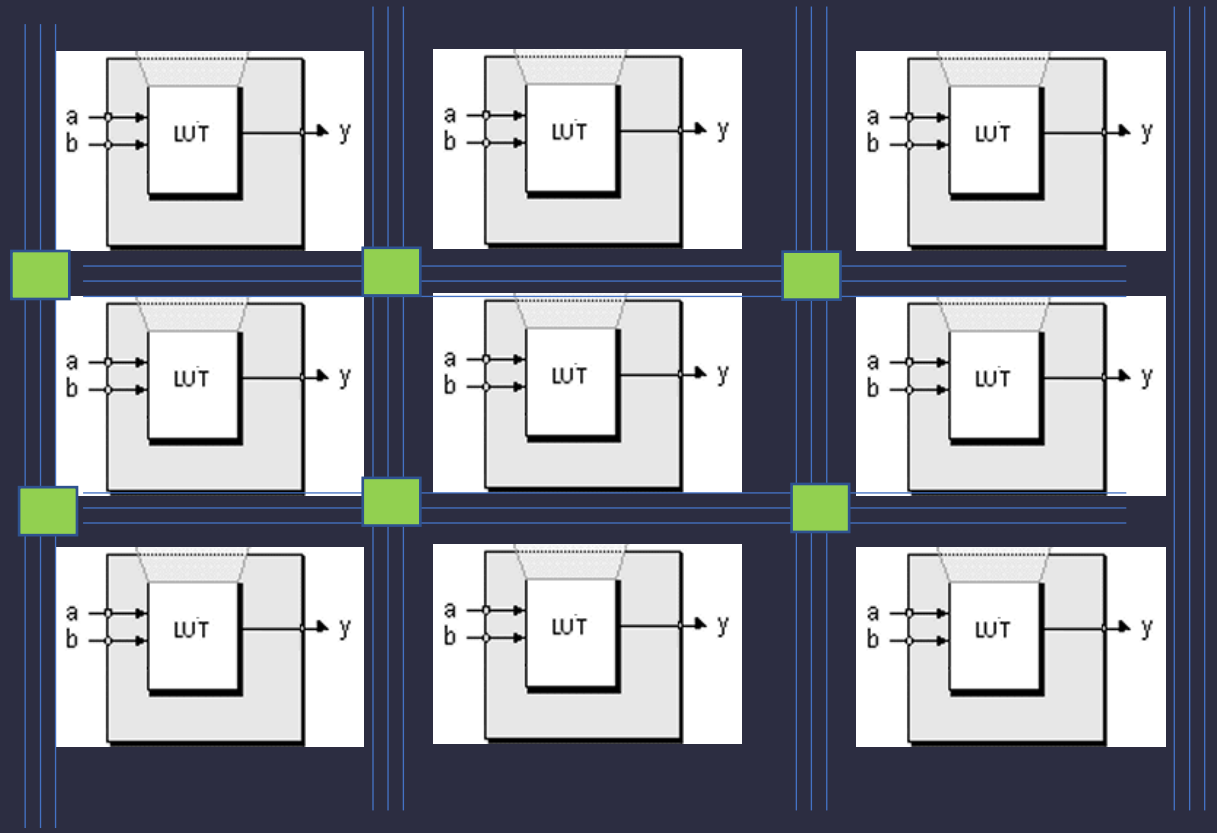
Verilog – Combinational Circuits

What is FPGA?



Verilog – Combinational Circuits

What is FPGA?



What is FPGA?

- FPGA (Field programmable Gate Arrays) is an integrated chip.
- It contains programmable blocks and configurable connections between these blocks.
- By programming these blocks and connections, the desired circuit can be implemented in the FPGA .

Example FPGA Chip

What is FPGA?

- Some FPGAs can only be programmed once.
- It is called one-time programmable (OTP).

What is FPGA?

- "Field Programmable" means that it can be programmed in the required application with unlimited count.

- This means that after the FPGA chips are produced in the factory, they can be used in the desired design later on.

Why is FPGA important?

Wide variety of integrated circuits (IC – Integrated circuits) are available.

- Memory
- Microprocessors
- Programmable logic devices (Programmable logic devices)
  - SPLD (Simple)
  - CPLD (Complex)
- ASIC – Application specific integrated circut
- And FPGAs ...

ASICs

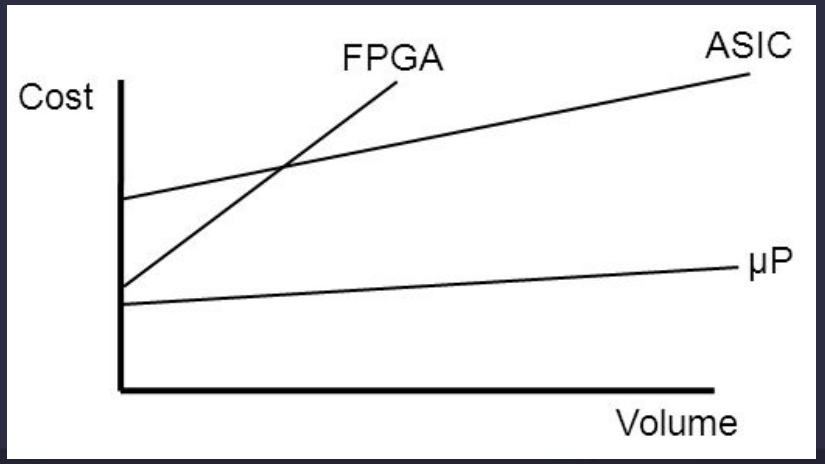
- They are useful in the implementation of huge and complex circuits.
- ASICs are integrated circuits built to perform a specific operation.
- ASICs provide very high performance (operation at high frequencies) , ASIC design complexity and design time and costs are quite high.
- And the produced chips cannot be modified . In case of a fault with the chip, all produced chips will be thrown away.

FPGAs

- FPGAs It is programmable.
- Unlike ASICs ; In the case of an error in the design, the design can be repeatedly modified and tested.

FPGAs

- FPGAs They are much cheaper than ASICs . (ASICs are only cheap when millions of units are produced)
- FPGAs is much easier than creating an ASIC design.
- Due to the shorter design time, once a product is produced, the time to market is shorter.
- NRE (Non-recurring engineering) is high when developing a ASIC Design



Chip Design Training

FPGA is mainly used

- Telecommunication
- Networking
- Automotive
- Medical
- Various industrial applications
- Prototypes of ASIC designs
- DSP (Digital signal processor) applications
- SoC (System on Chip), a single IC where all necessary electronics are gathered together

Reasons for FPGA Use

- Computing Power
- Controlling with nanosecond order

Reasons for FPGA Use

Processors

```
c[0]=a[0]+b[0];
c[1]=a[1]+b[1];
c[2]=a[2]+b[2];
c[3]=a[3]+b[3];
...
c[1000]=a[1000]+b[1000];
```

FPGA

```
c[0]<=a[0]+b[0];
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Reasons for FPGA Use

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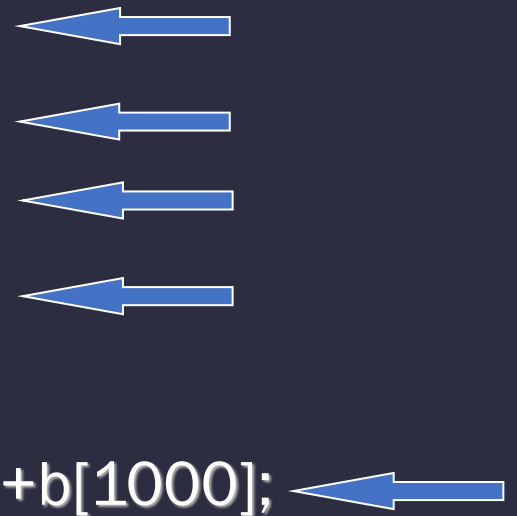
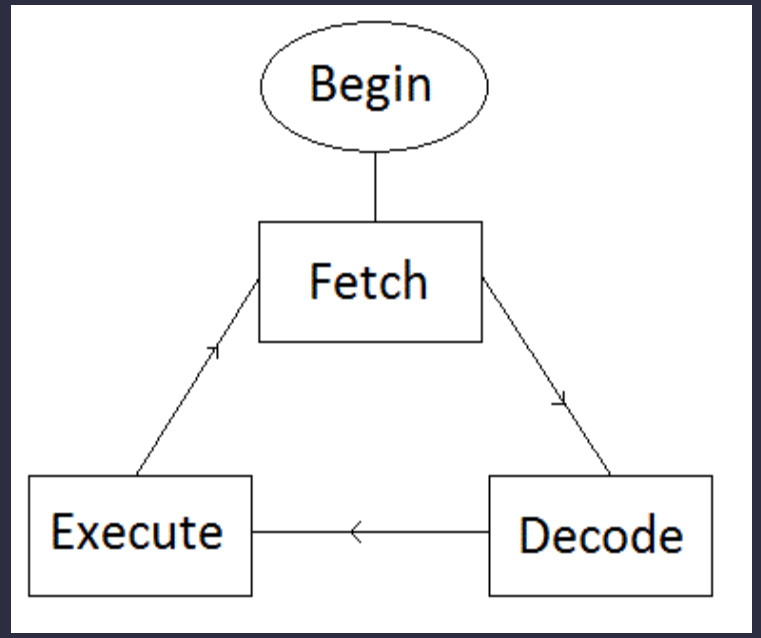
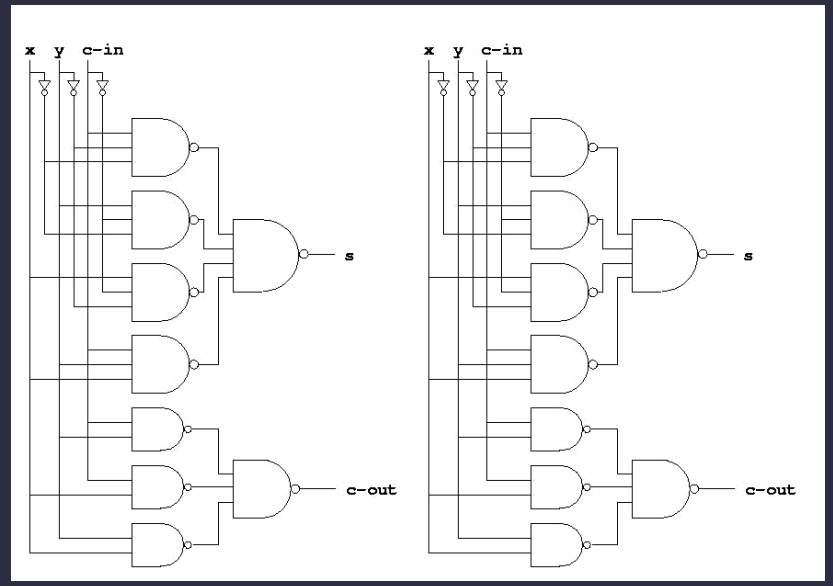


Reasons for FPGA Use

Processors



FPGA



Reasons for FPGA Use

CPU

For 1000 transactions (assume each operation takes 1 cycle),

Average Processor frequency: 3 GHz,

Required Time = Number of operations X (1/Frequency)

= 1000 X 1/3 billion

= 333 nanoseconds

FPGA

For 1000 transactions (assume each operation takes 1 cycle),

Average FPGA frequency: 100mhz

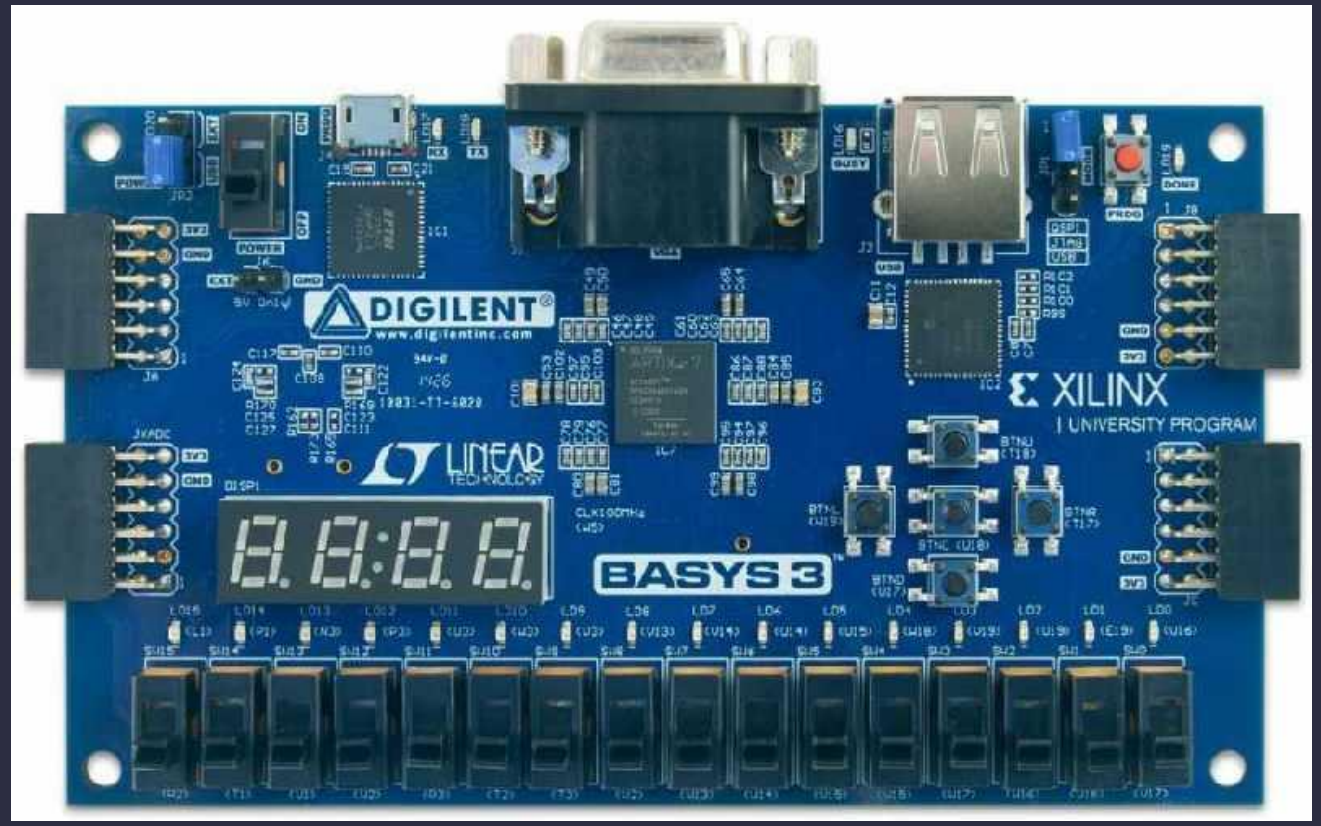
Time required = 1 x (1/Frequency)

= 1 X 1/100m

= 10 nanoseconds

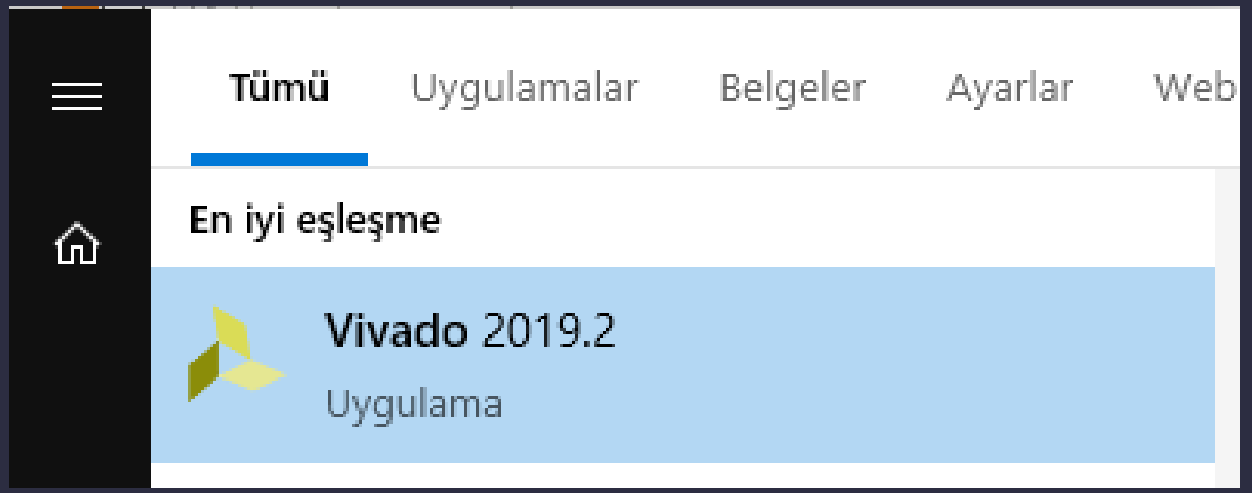
Verilog – Combinational Circuits

In LABs Xilinx Basys3 FPGAs with Artix 7 FPGAs will be used.



Verilog – Combinational Circuits

Vivado IDE will be used to programming Xilinx Based FPGAs



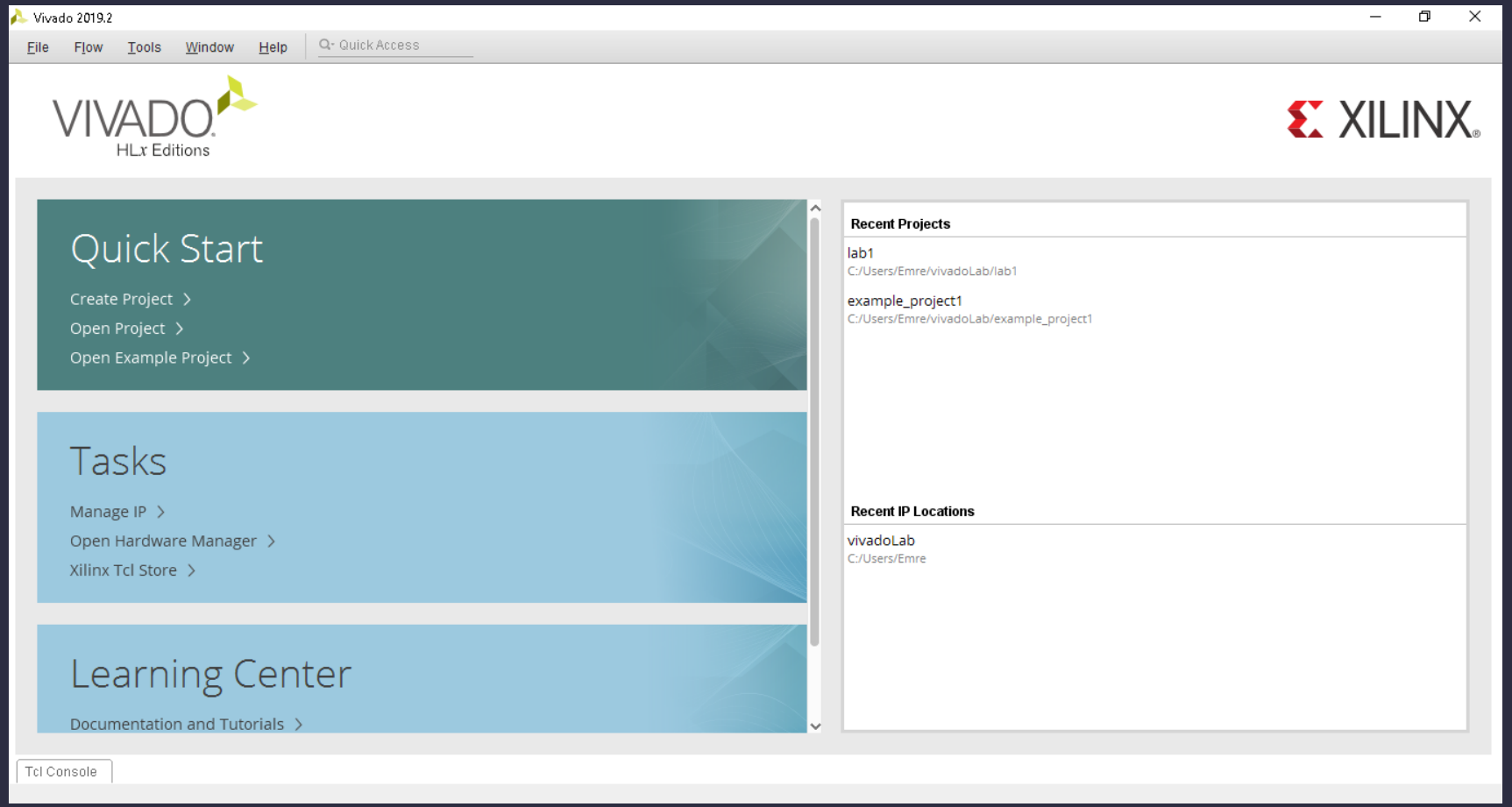
Verilog – Combinational Circuits

Vivado Design Tool

- Download Address: https://www.xilinx.com/support/download.html
- Installation and Licensing Video : https://www.youtube.com/watch?v=yW7t28XaVEs

Verilog – Combinational Circuits

Vivado Design Tool



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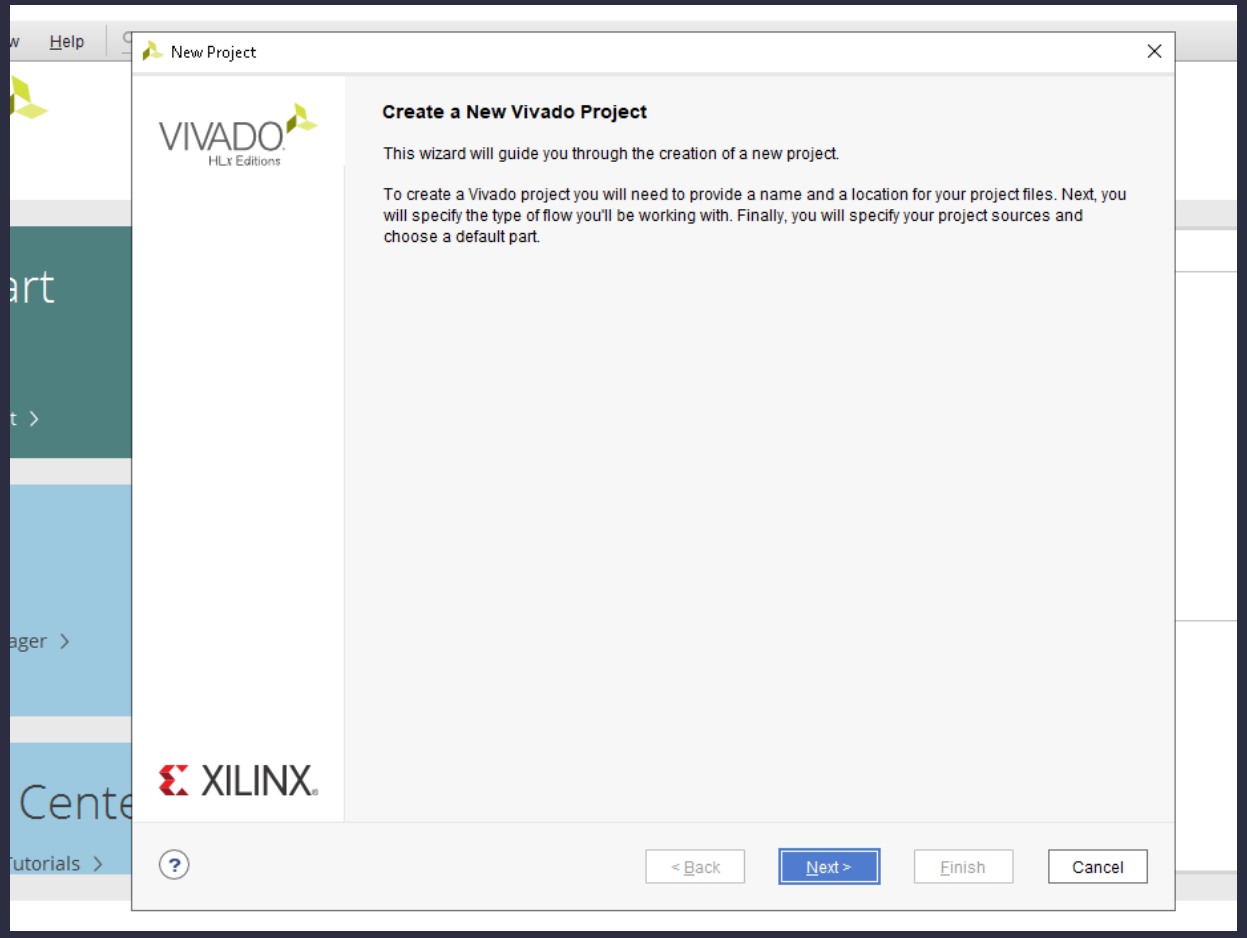

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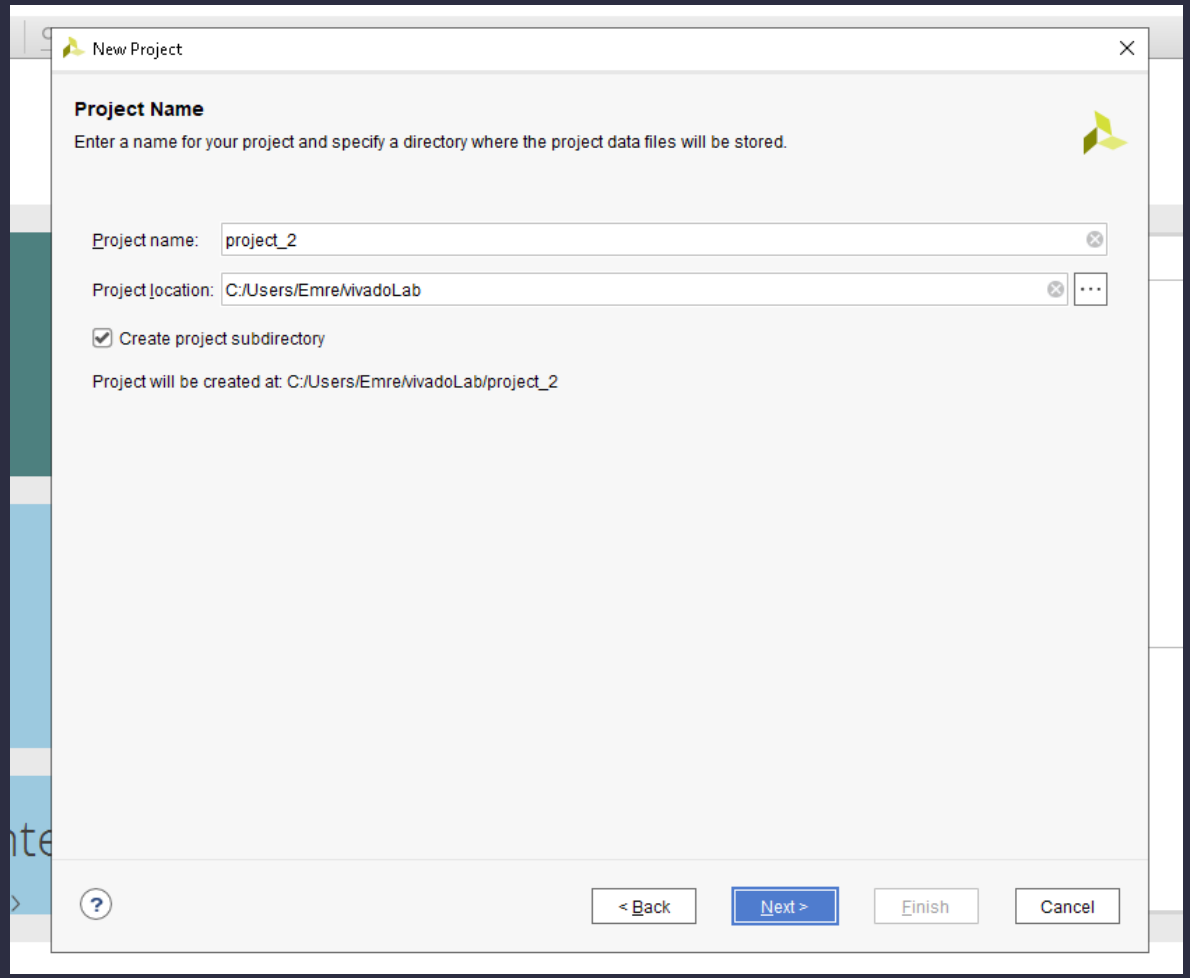

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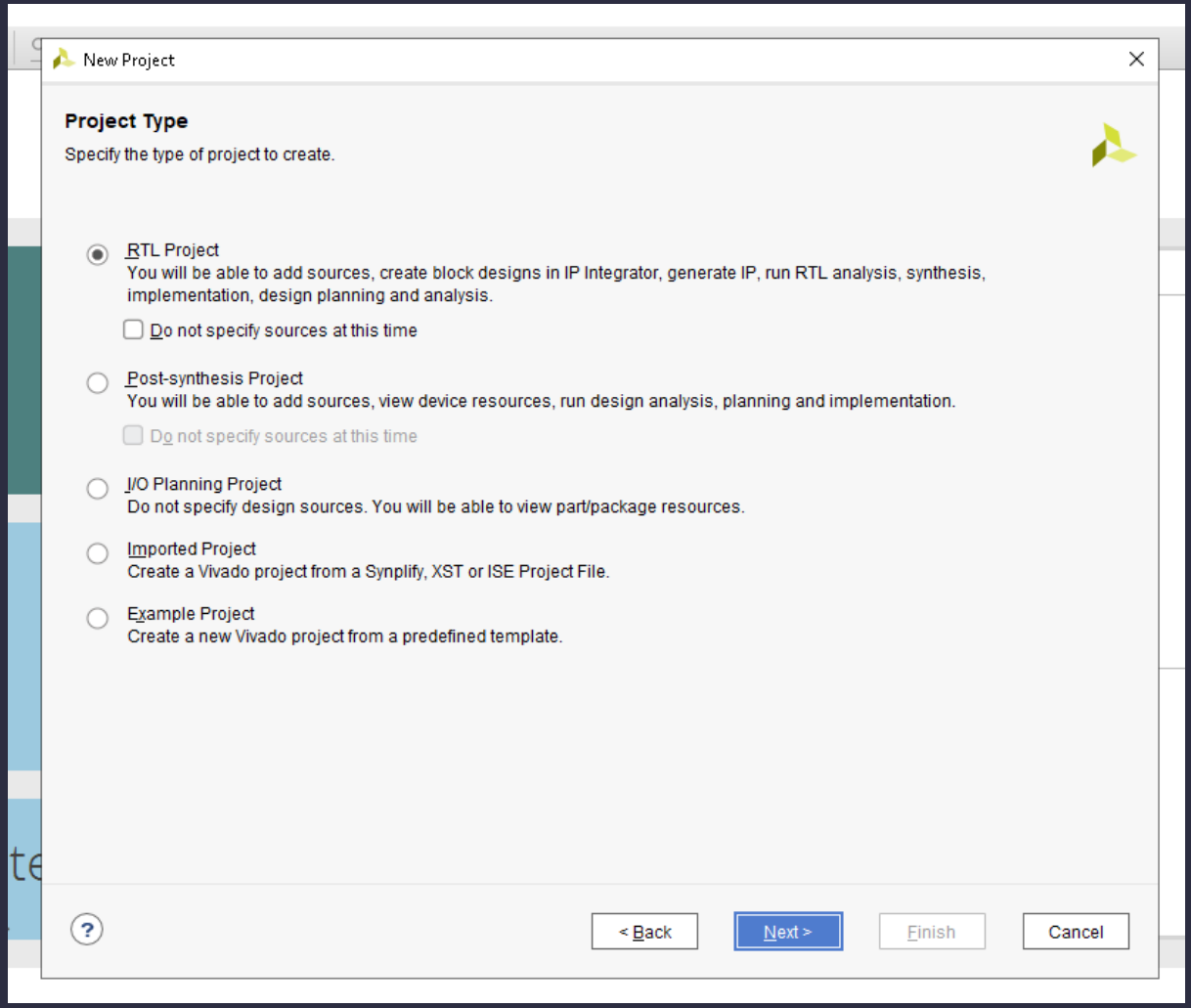

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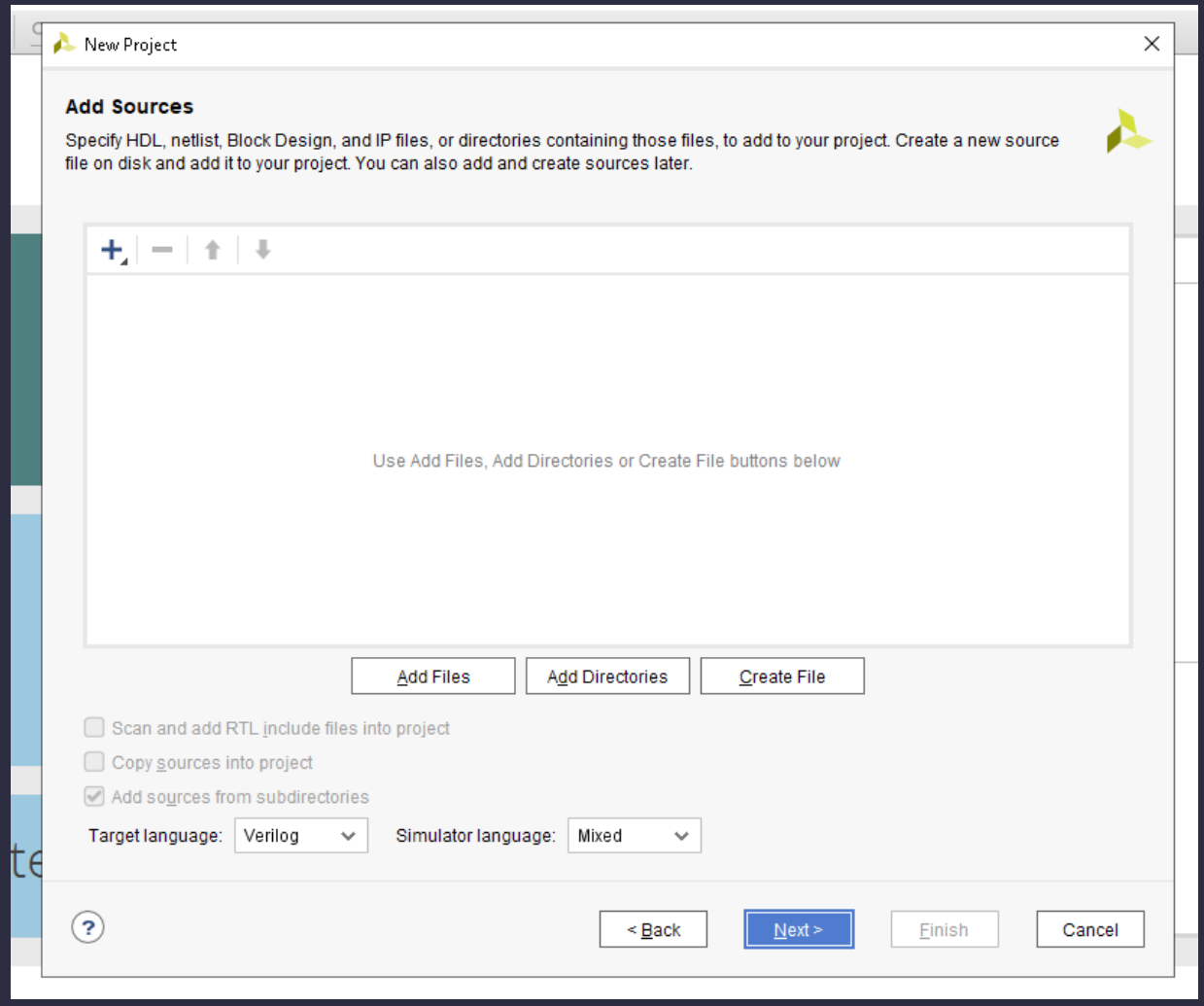

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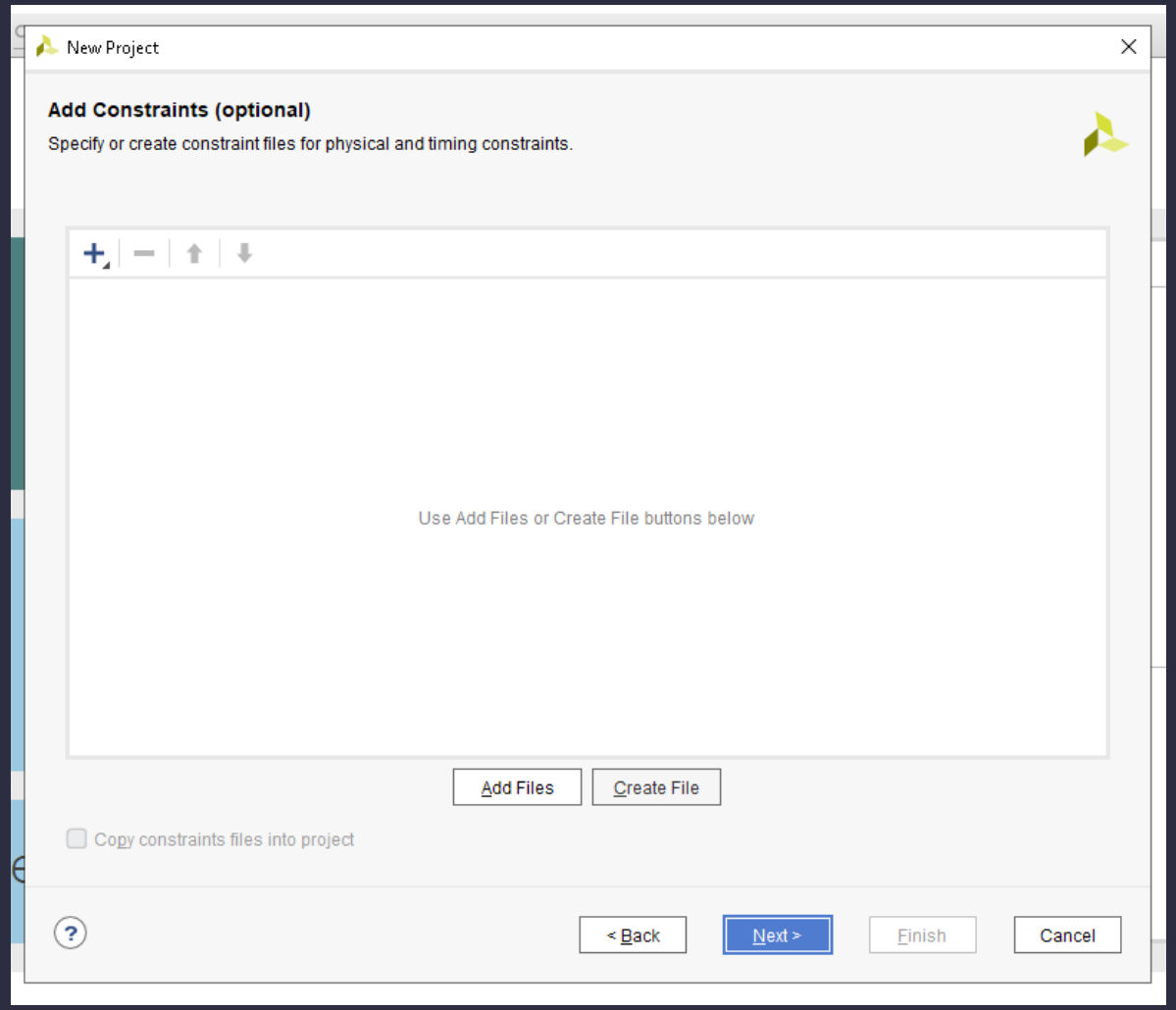


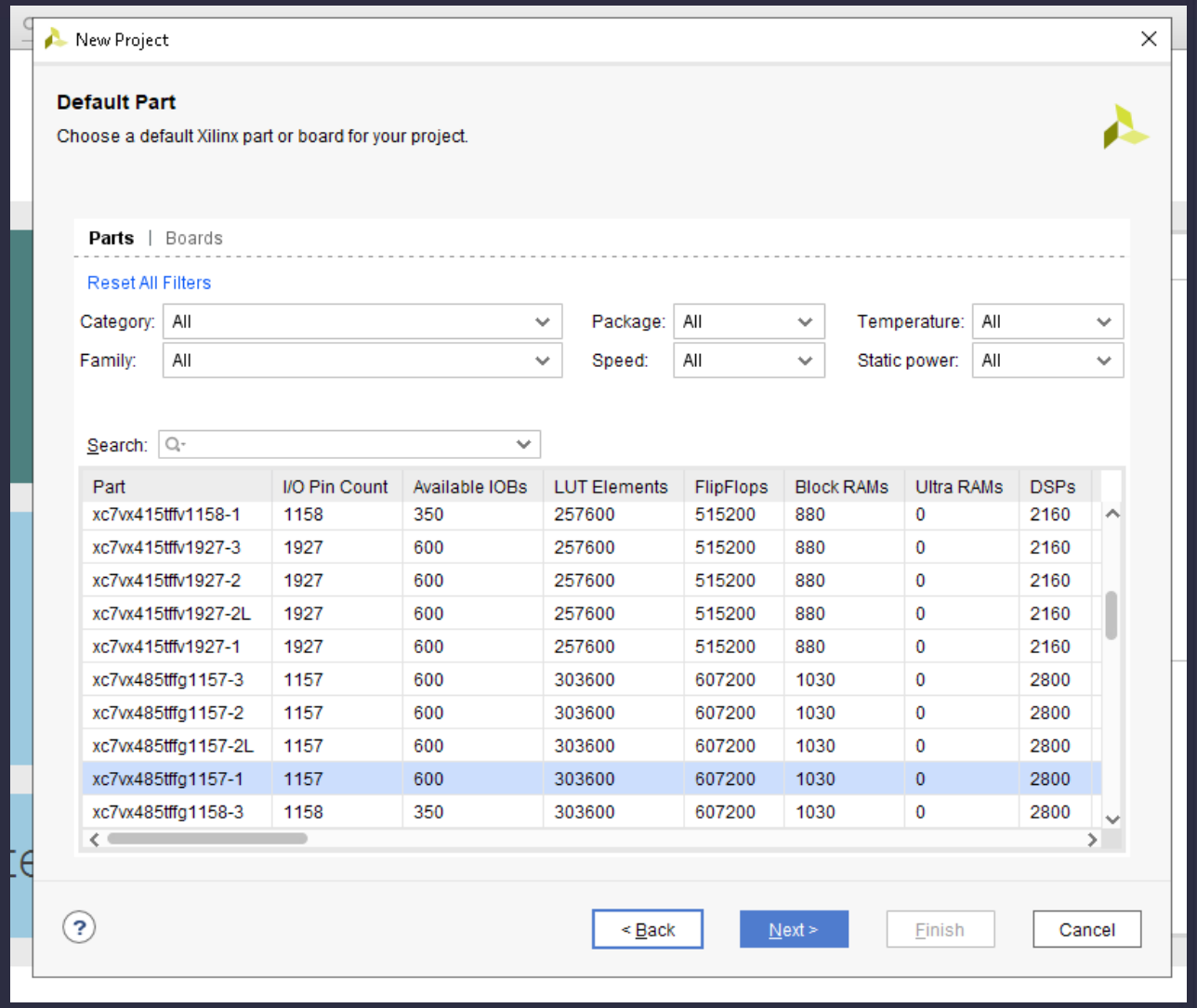
Verilog – Combinational Circuits

Vivado Design Tool

is the FPGA we will use in LABs

XC7A35Tcpg236-1

The model must be selected.



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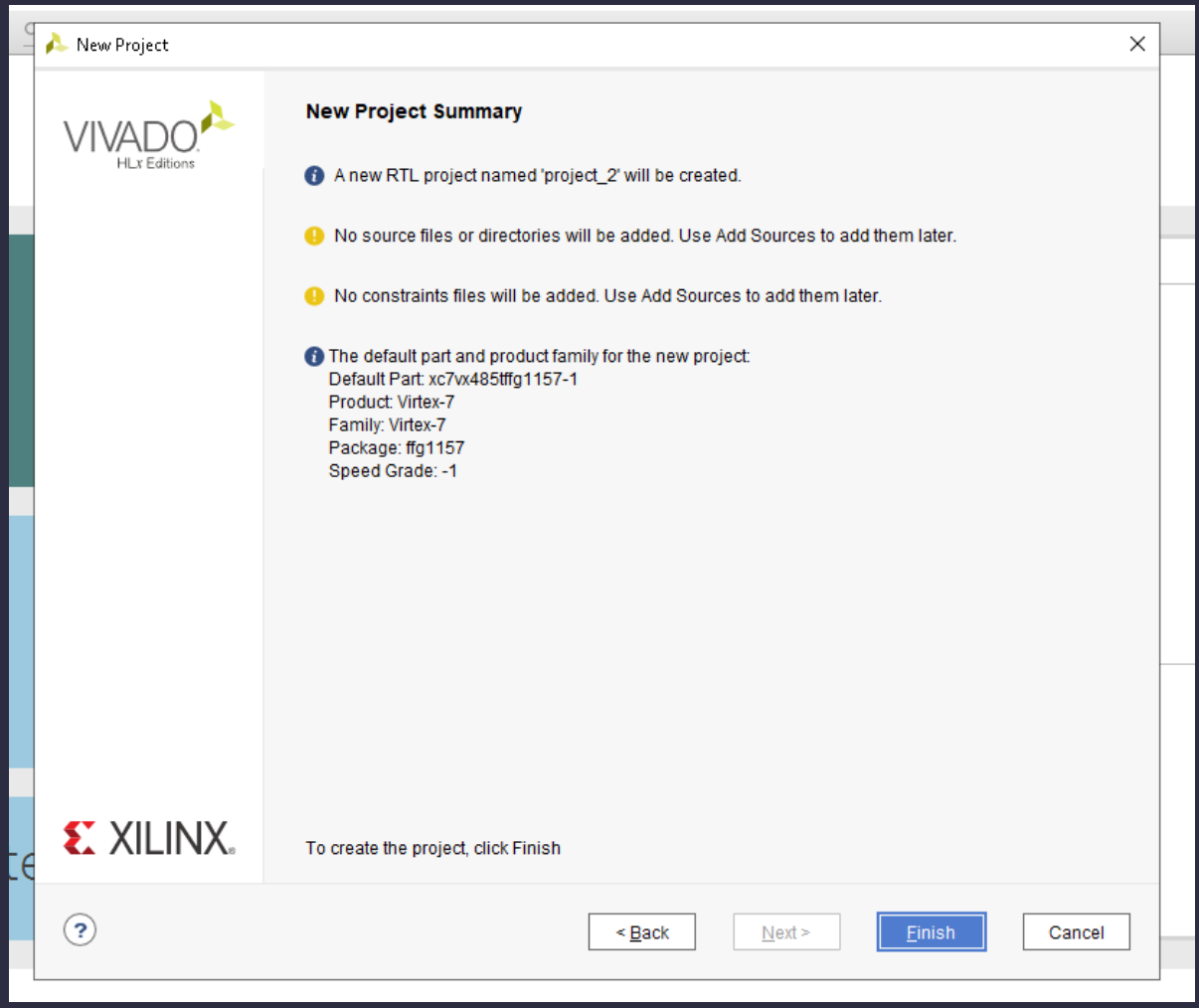
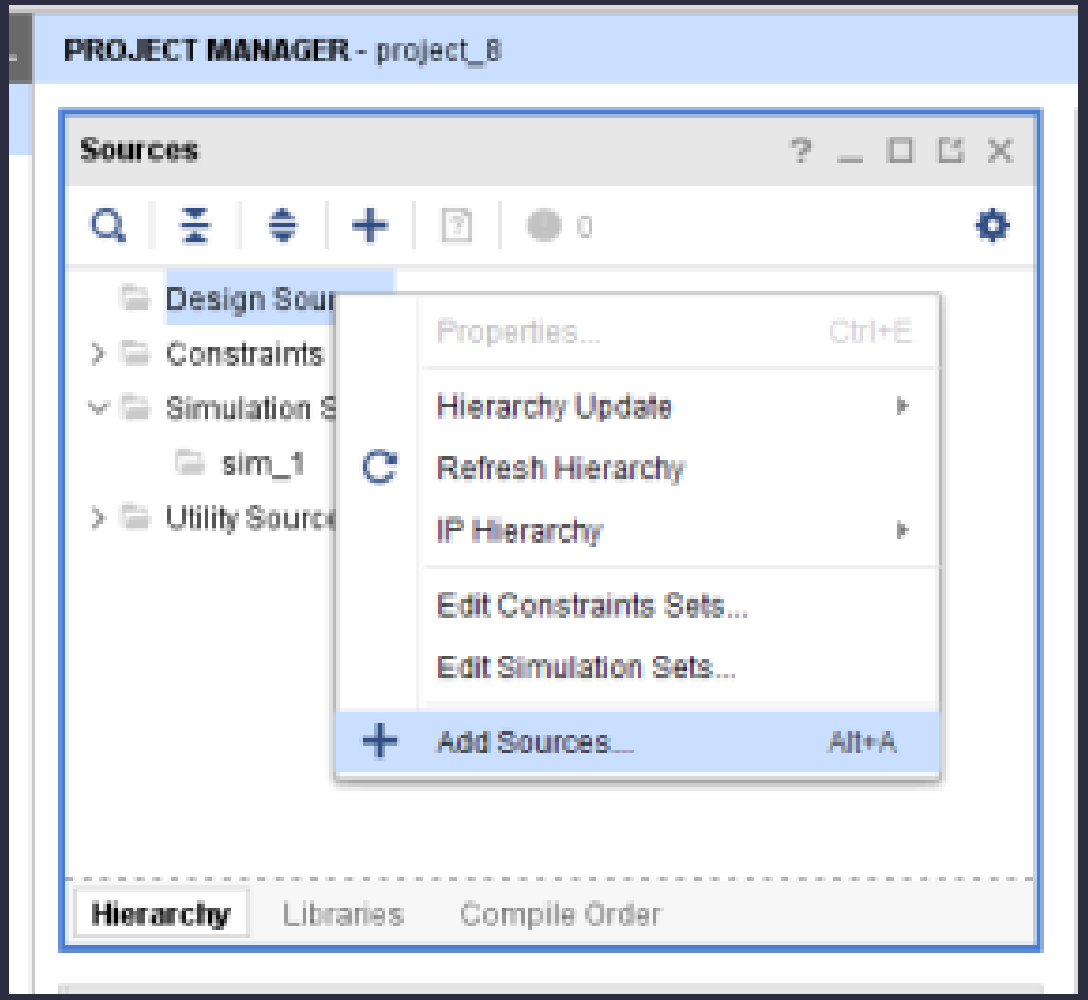
Vivado Design Tool



Verilog – Combinational Circuits

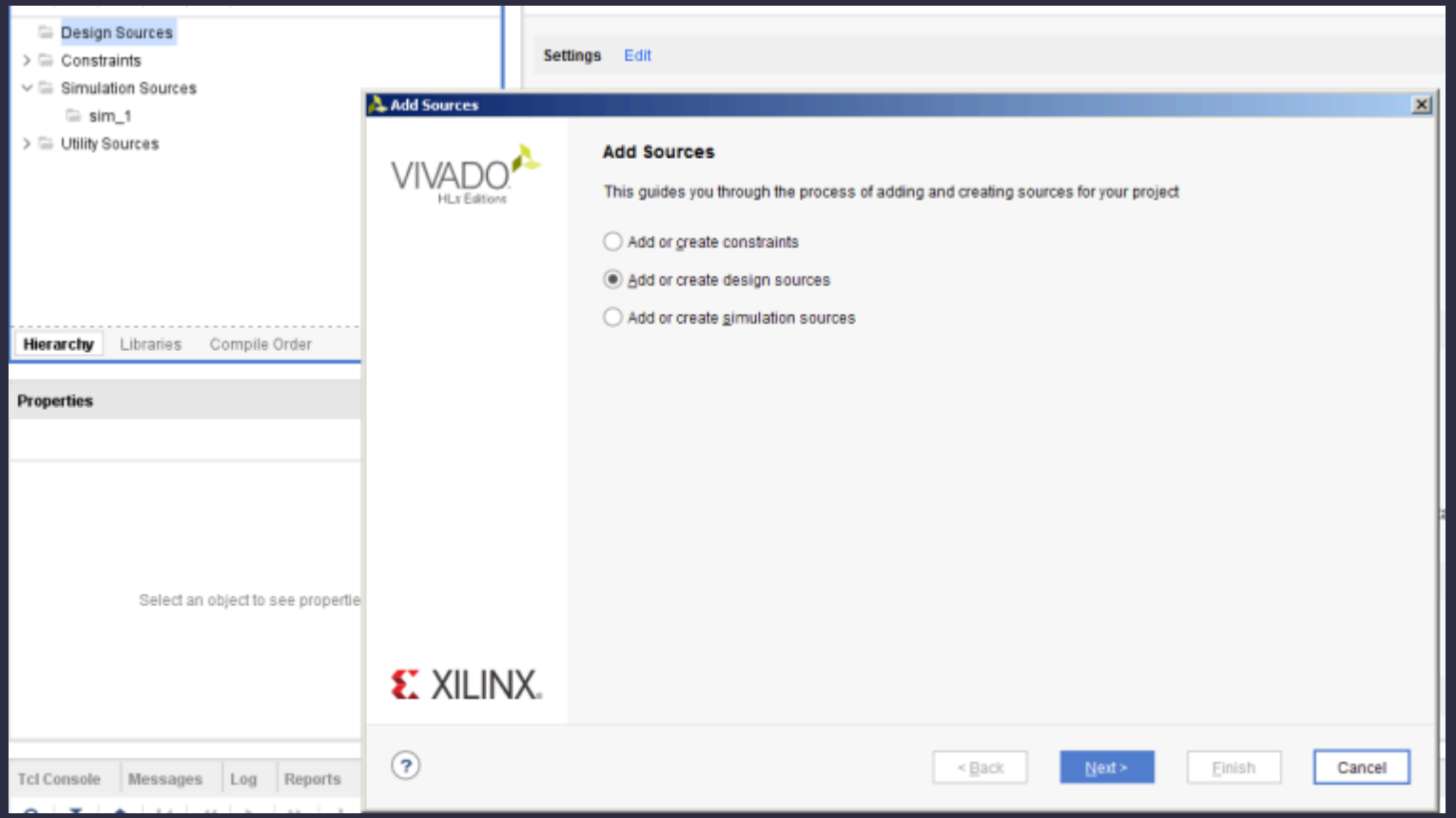
Vivado Design Tool

Adding a new design resource



Verilog – Combinational Circuits

Vivado Design Tool



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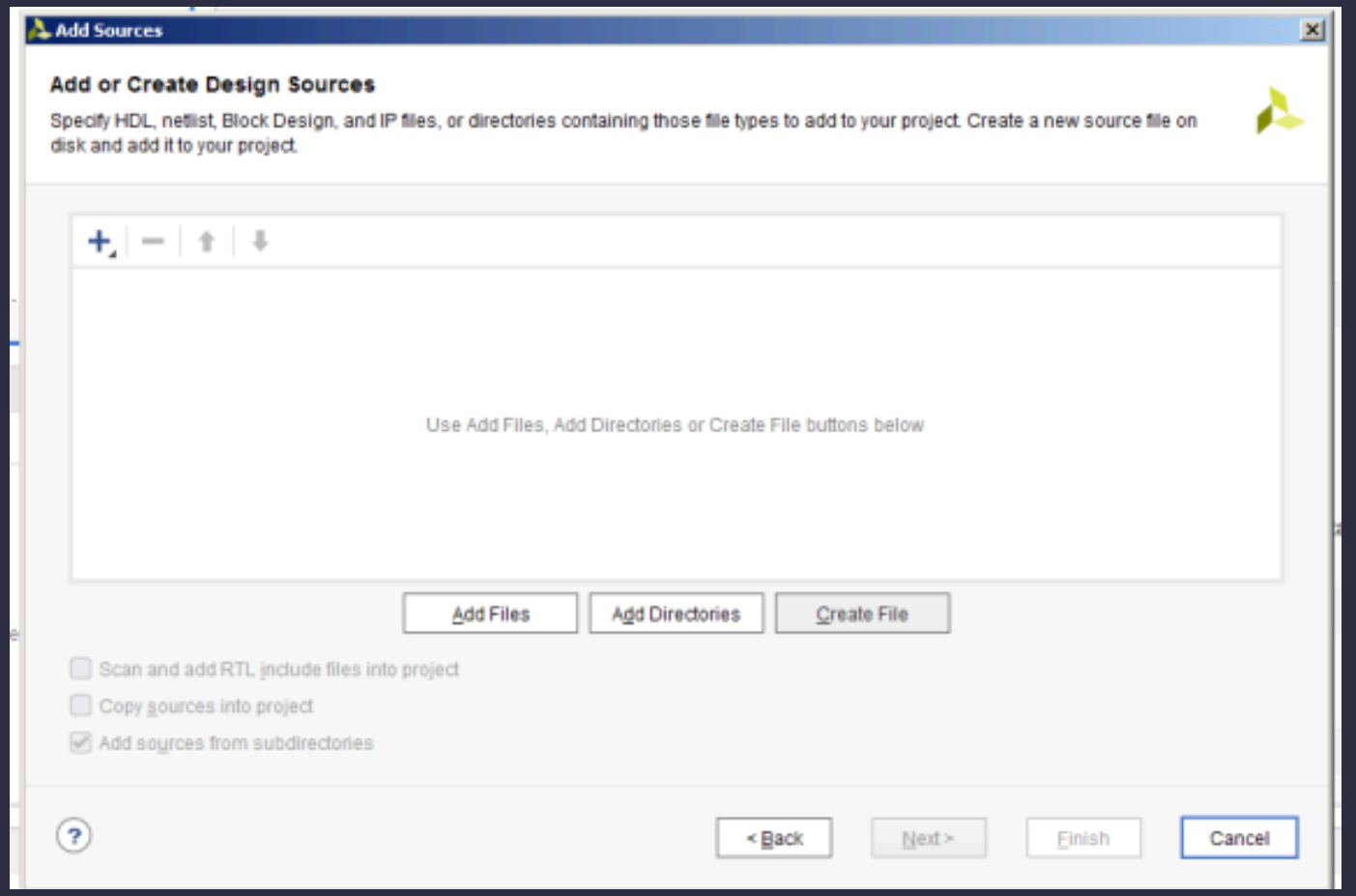

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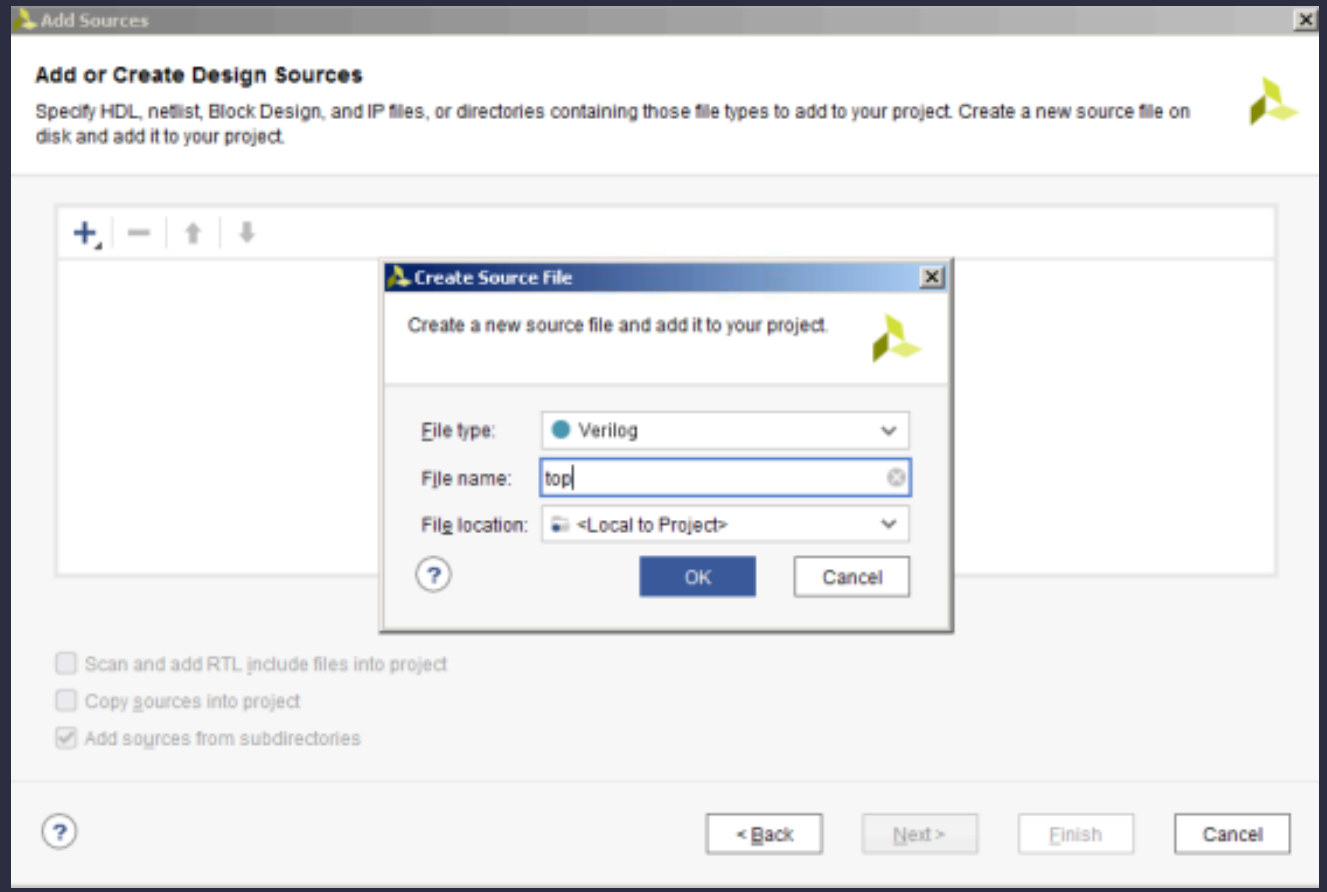

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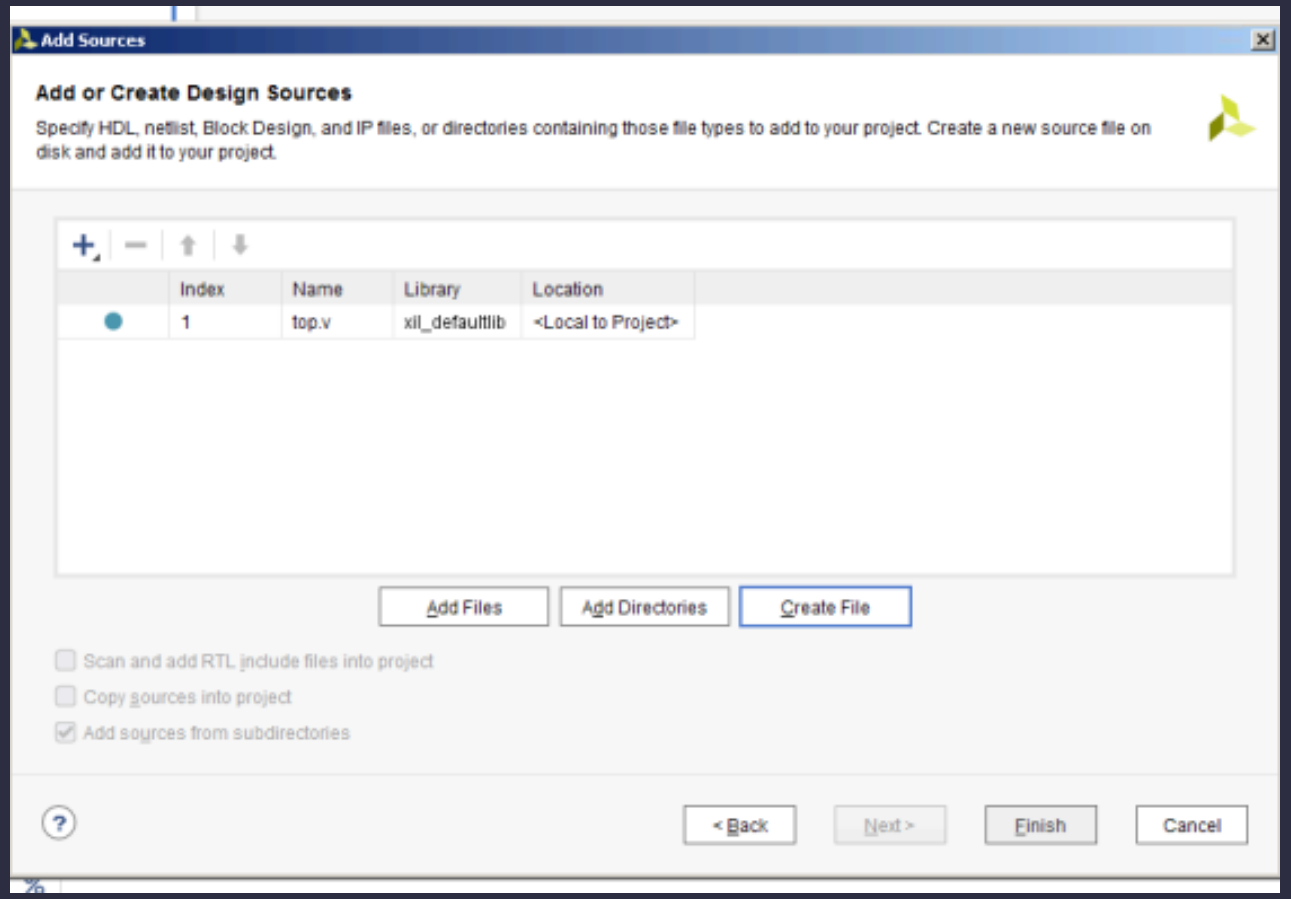
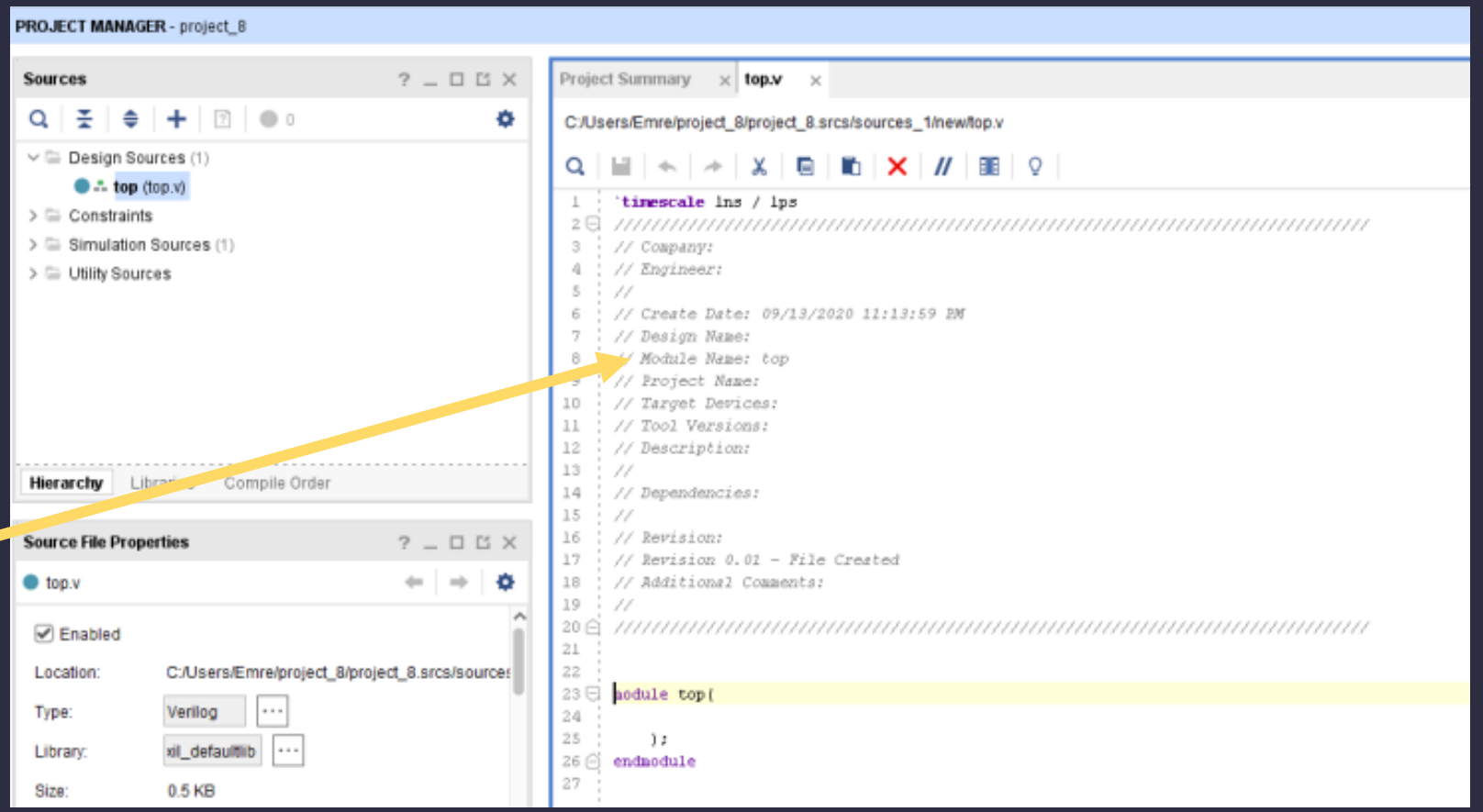


Verilog – Combinational Circuits

Vivado Design Tool

RTL Design

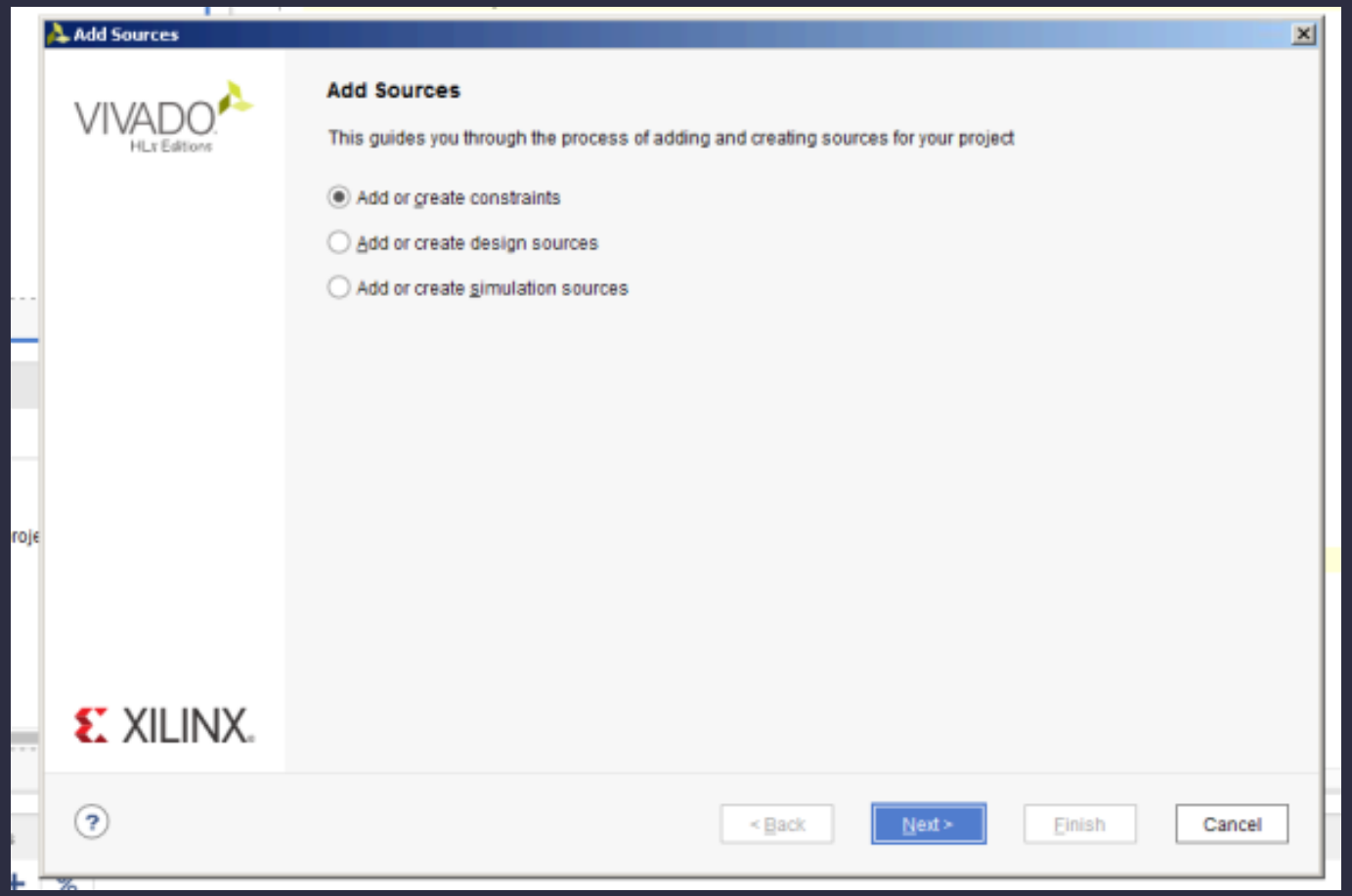
File To Do



Verilog – Combinational Circuits

Vivado Design Tool

Adding a constraint



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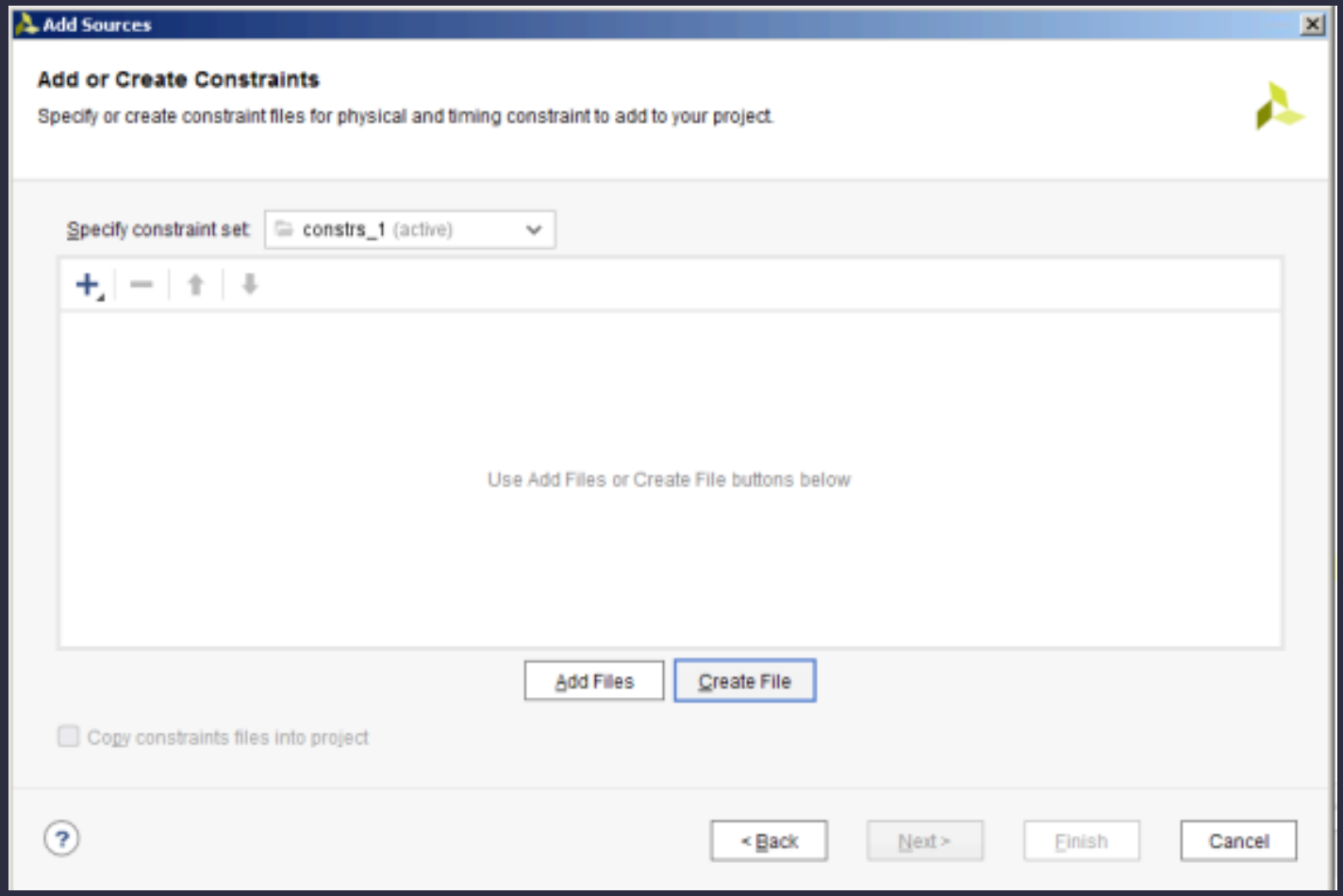

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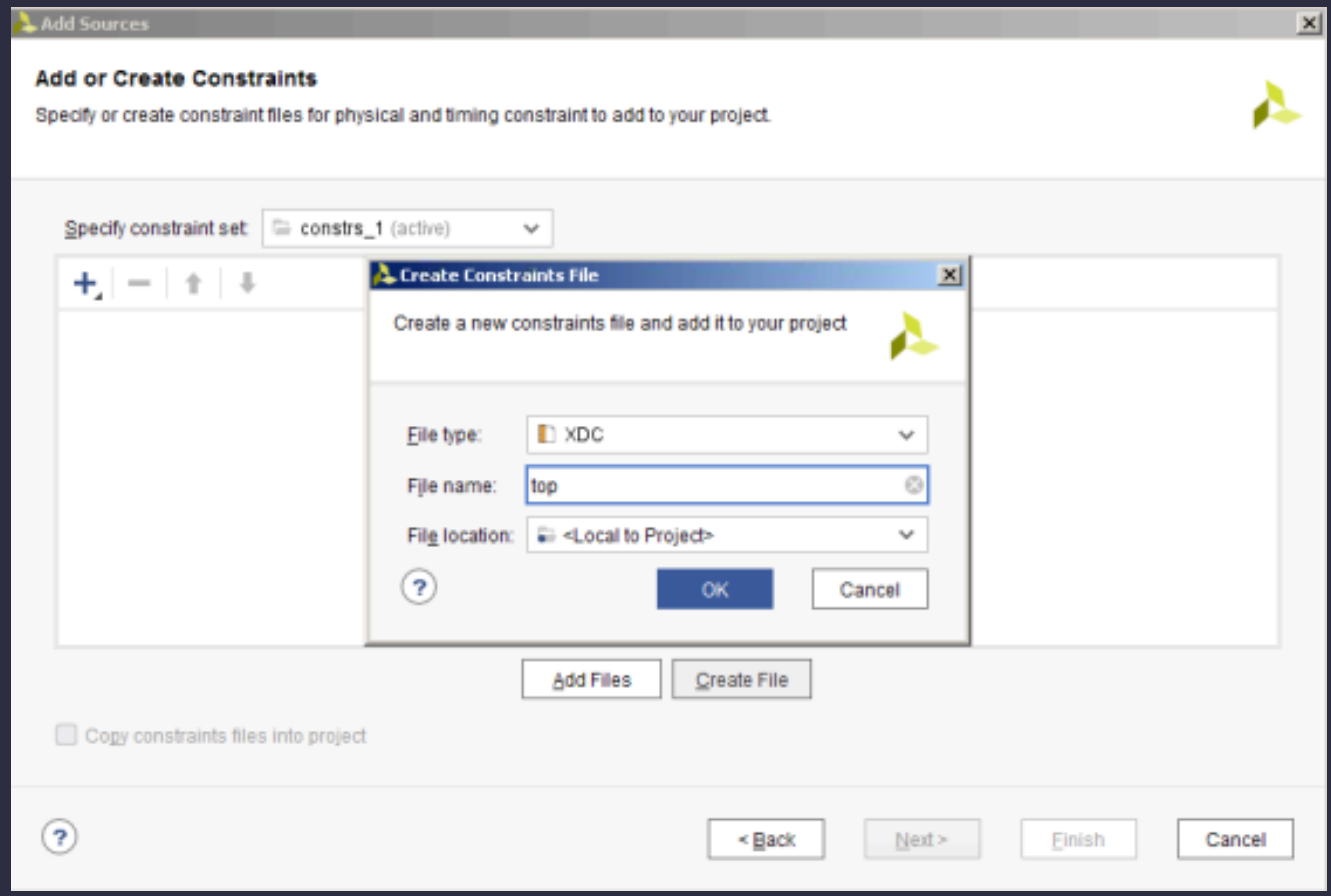

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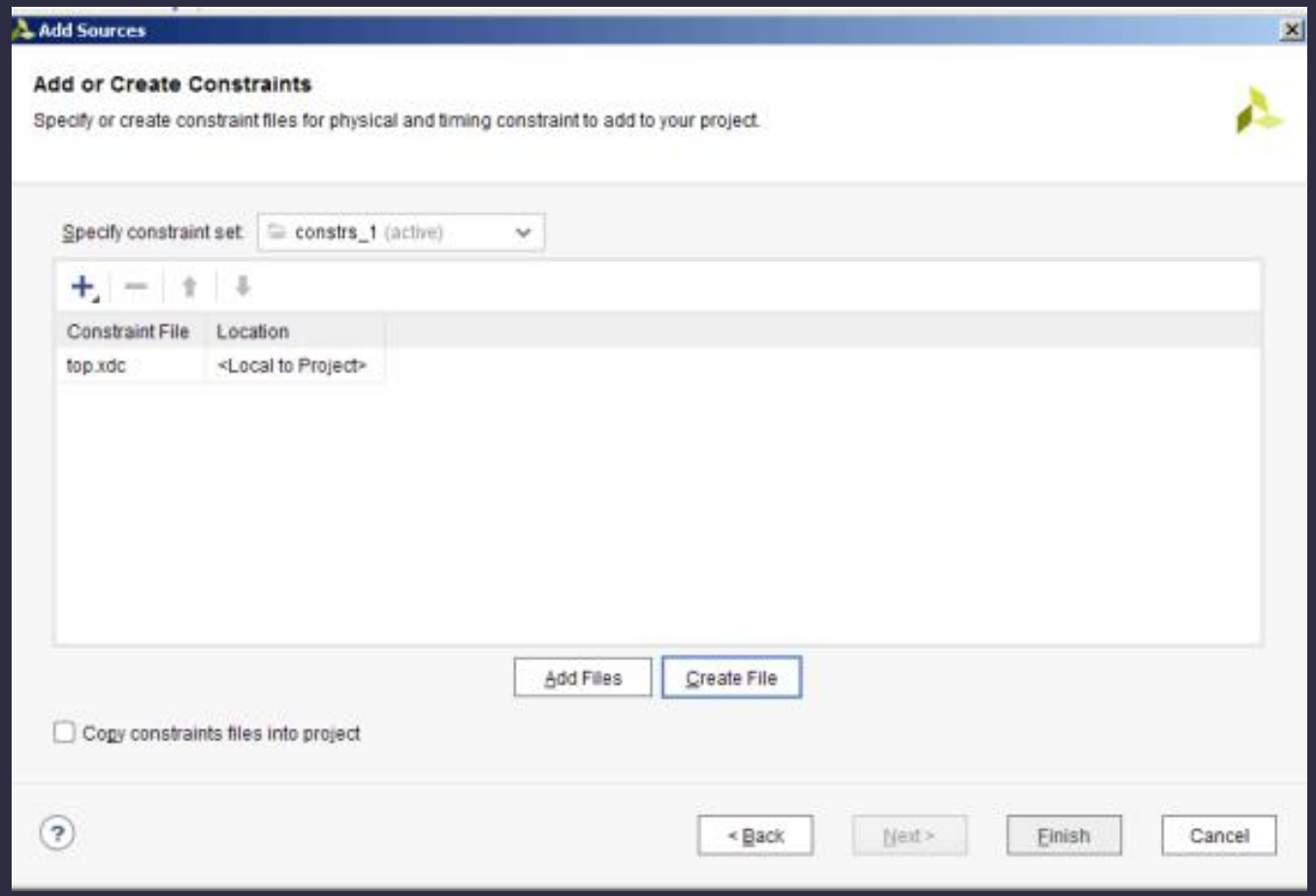

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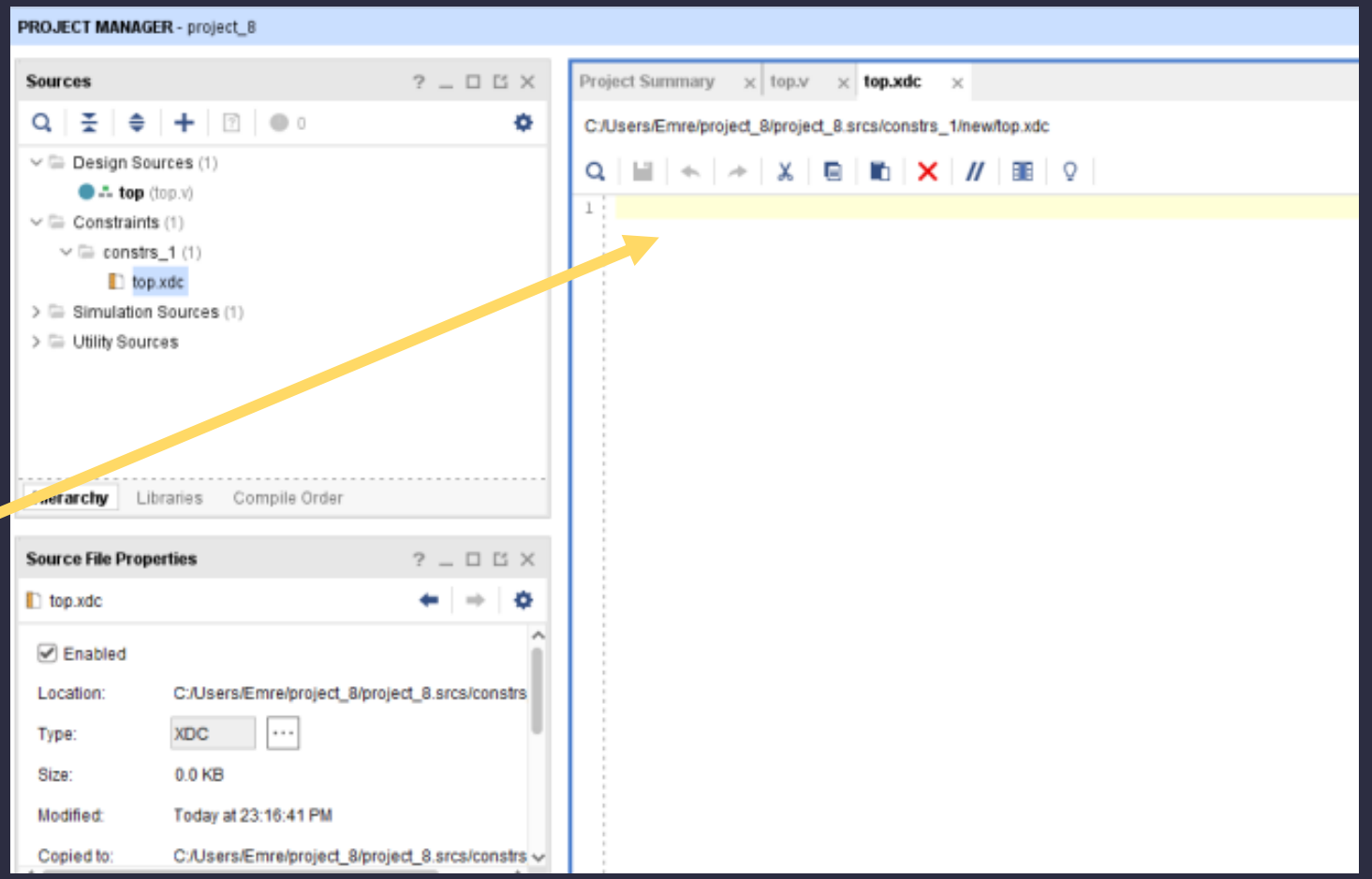
Vivado Design Tool

Adding a constraint

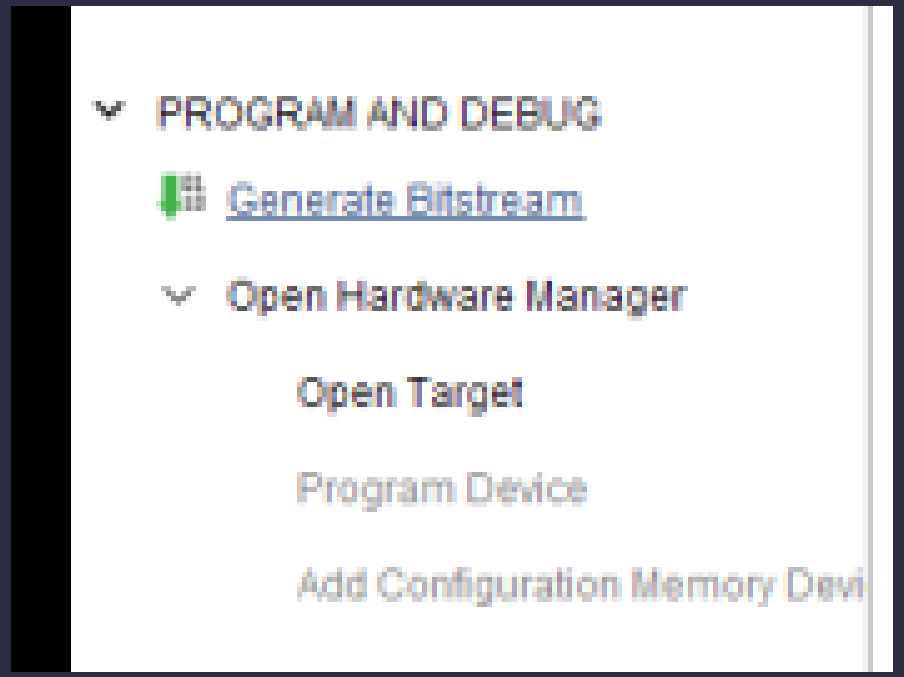
Write constraints



Verilog – Combinational Circuits

Vivado Design Tool

Bitstream generation



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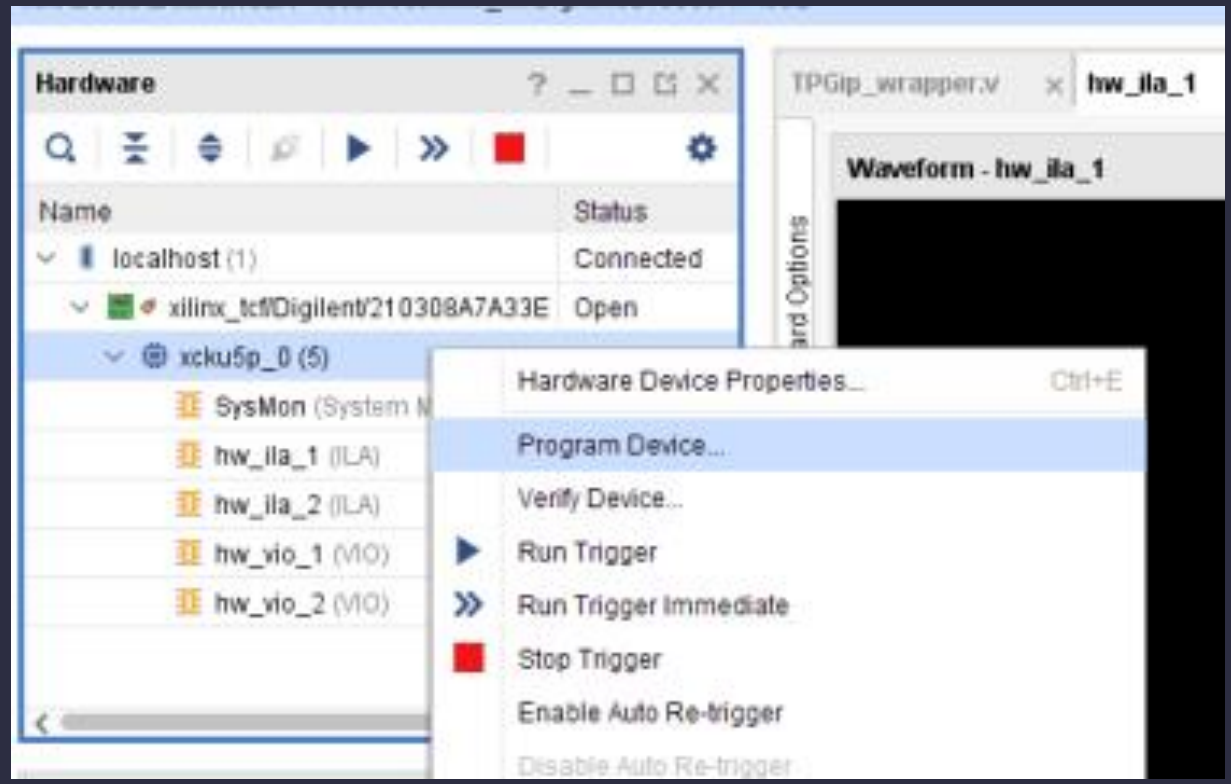

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