Digital Design

Week 3: Combinational Logic
Part IV

Fenerbahce University

Combinational Circuits

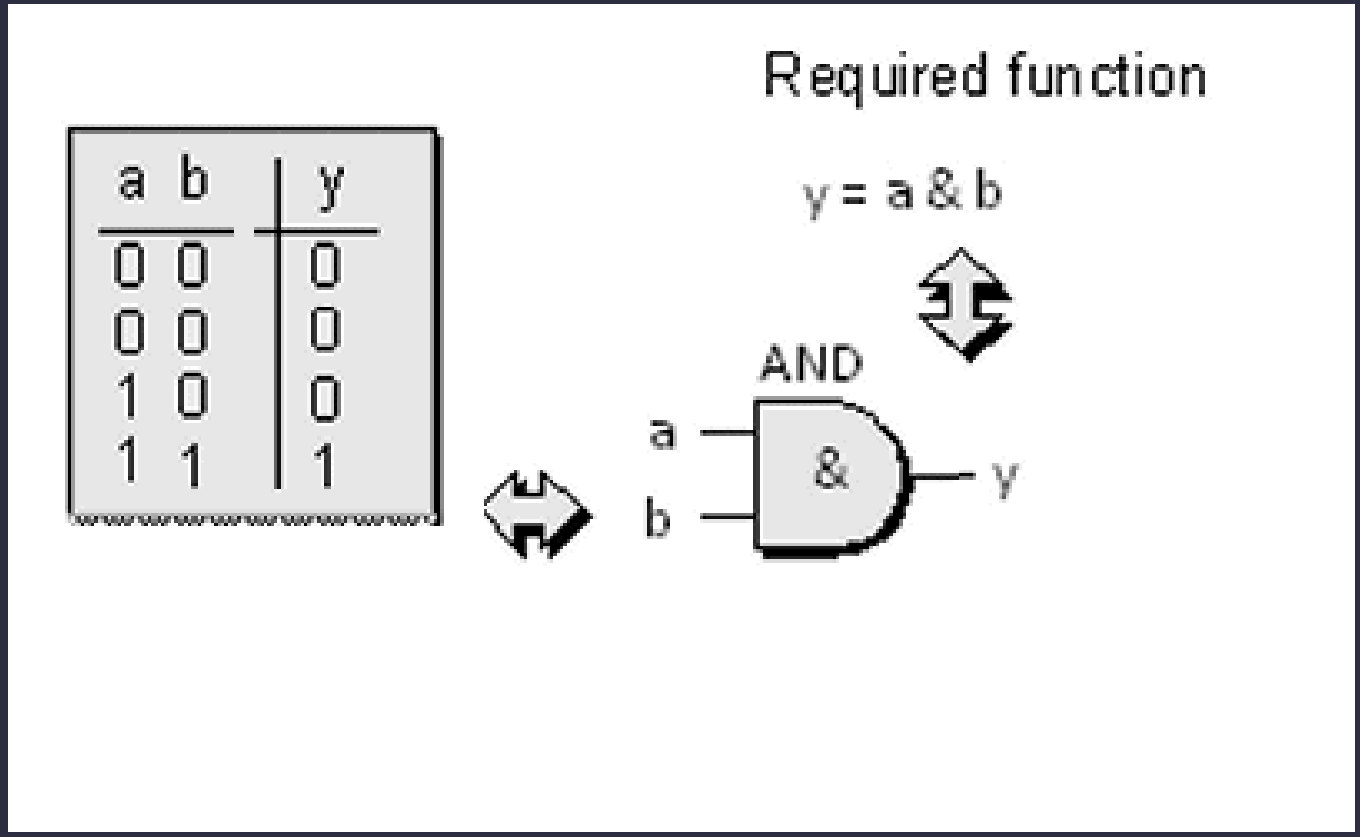
- Combinational Circuits
  - Introduction to Verilog

Verilog – Combinational Circuits

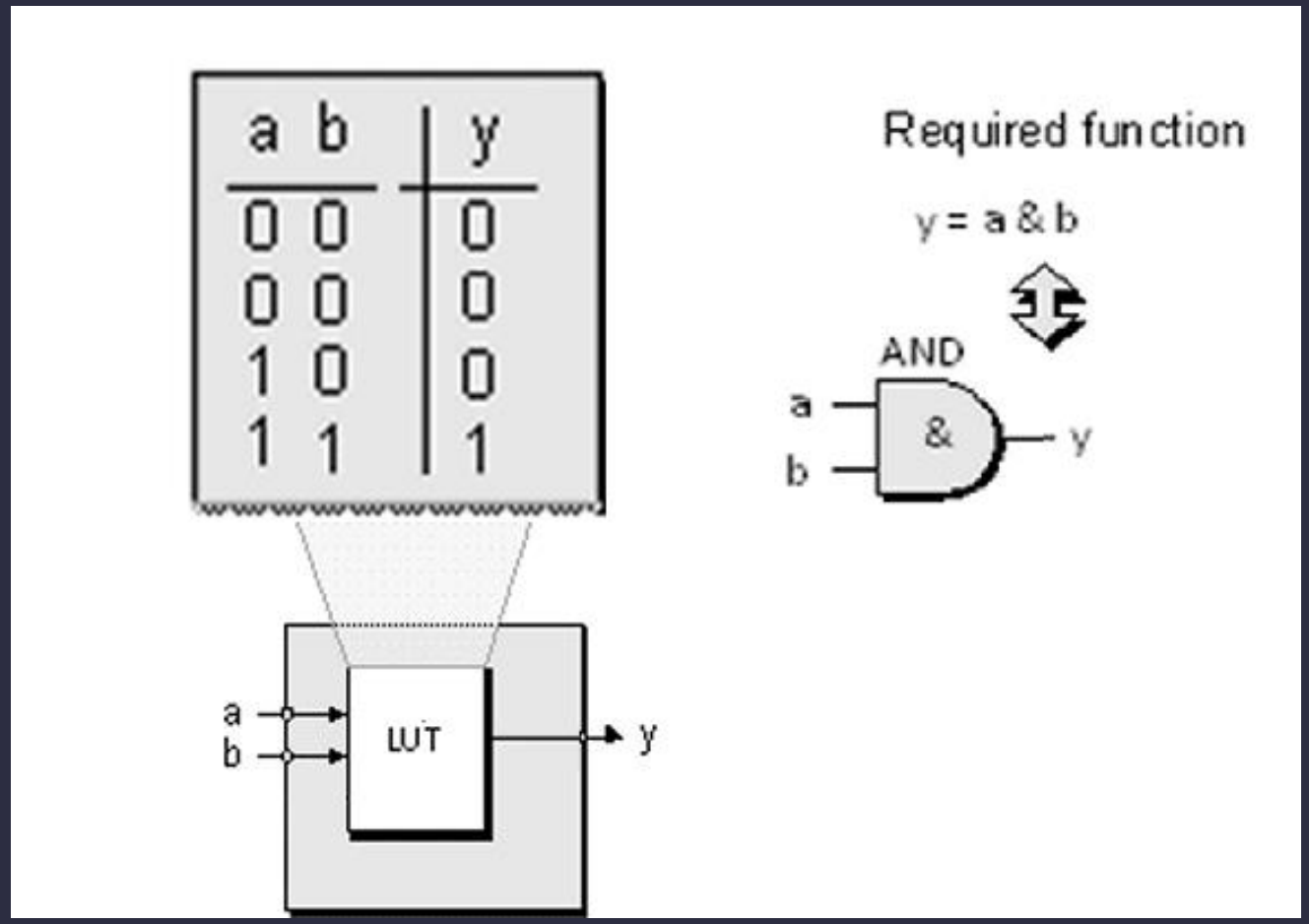
Most commonly using HDL (Hardware Description Language) Languages

- *Verilog*
- *System Verilog*
- *VHDL*

Verilog – Combinational Circuits



Verilog – Combinational Circuits



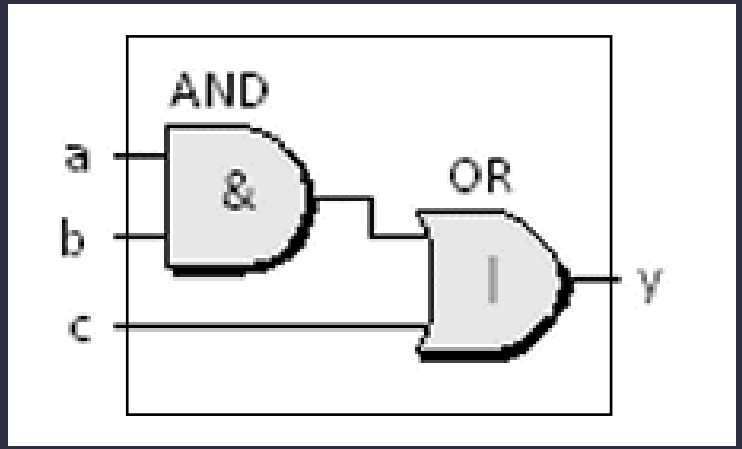
Verilog – Combinational Circuits

Vivado ,

- Verilog
- system Verilog
- VHDL

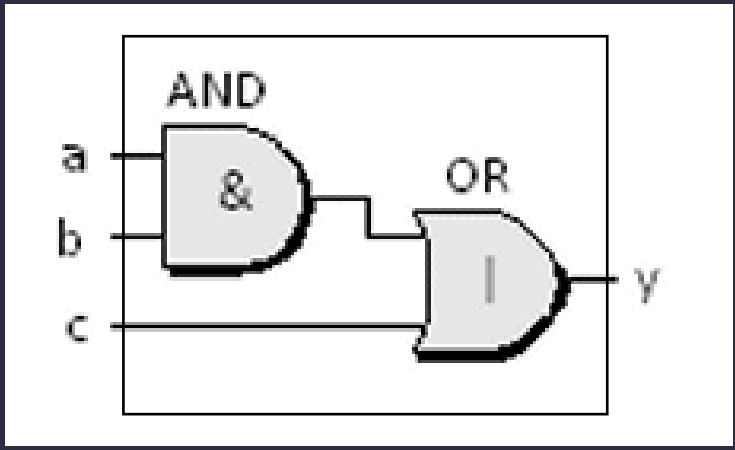
It supports languages. Within the scope of the course, designs will be made with Verilog language.

Verilog – Combinational Circuits



myModule

Verilog – Combinational Circuits



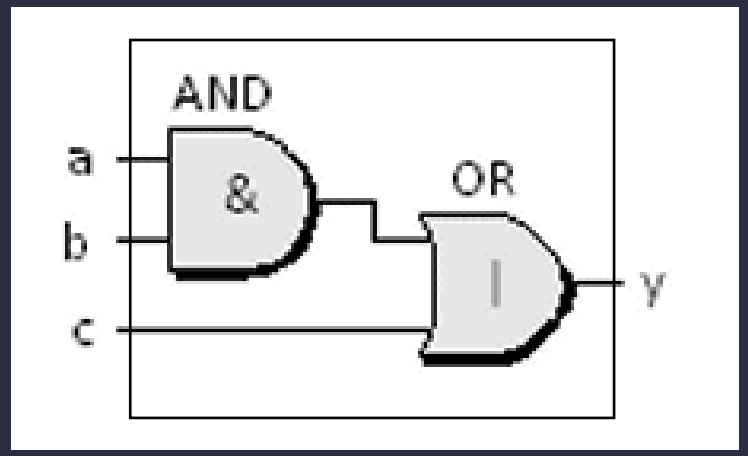
myModule

Verilog Design

```
module myModule ( input a, input b, output y);


endmodule
```

Verilog – Combinational Circuits



myModule

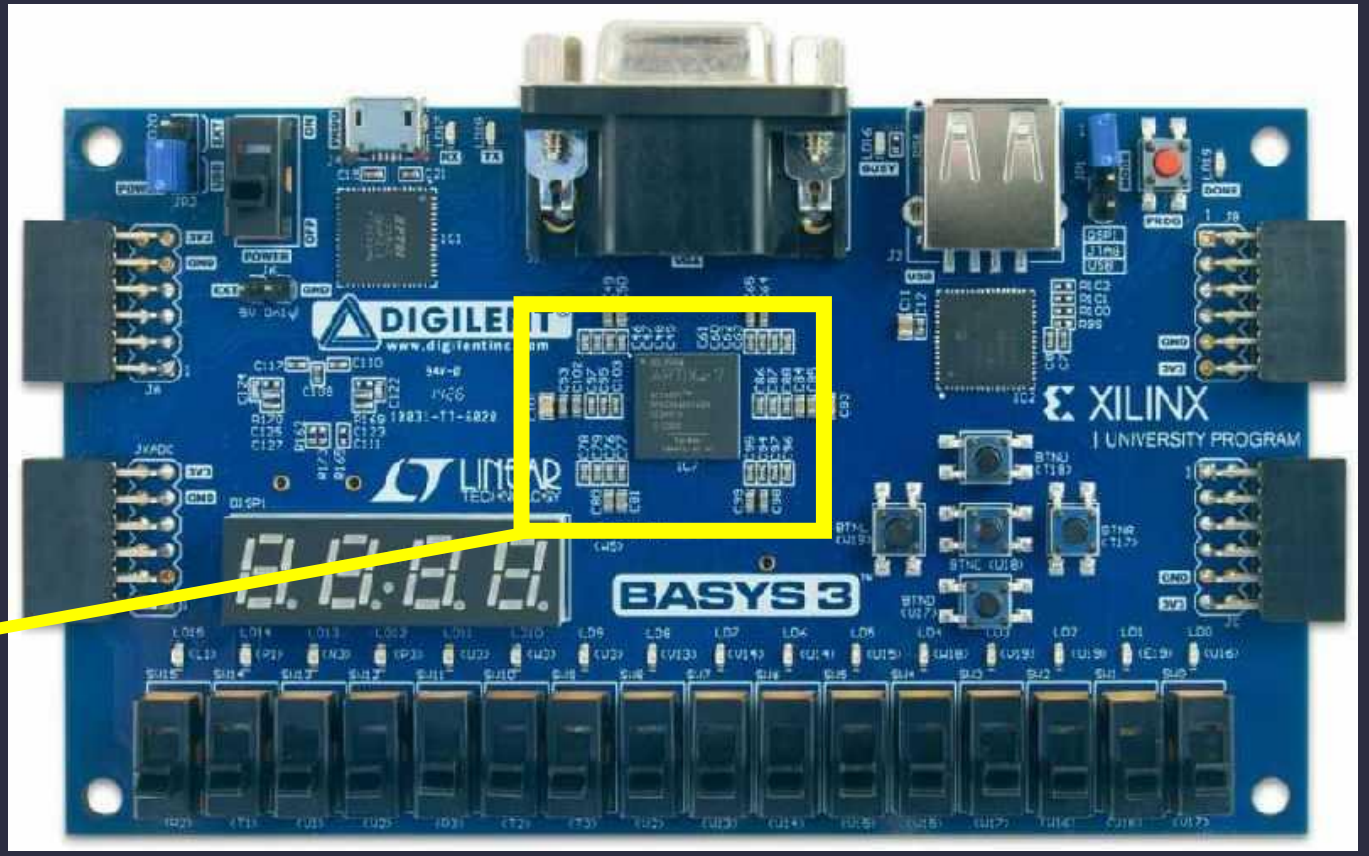
Verilog Design

```
module myModule(input  a, input b, output y);

        reg tmp;
        always@(*) begin
                tmp = a & b;
                y = tmp | c;
        end

endmodule
```

Verilog – Combinational Circuits



Verilog – Combinational Circuits

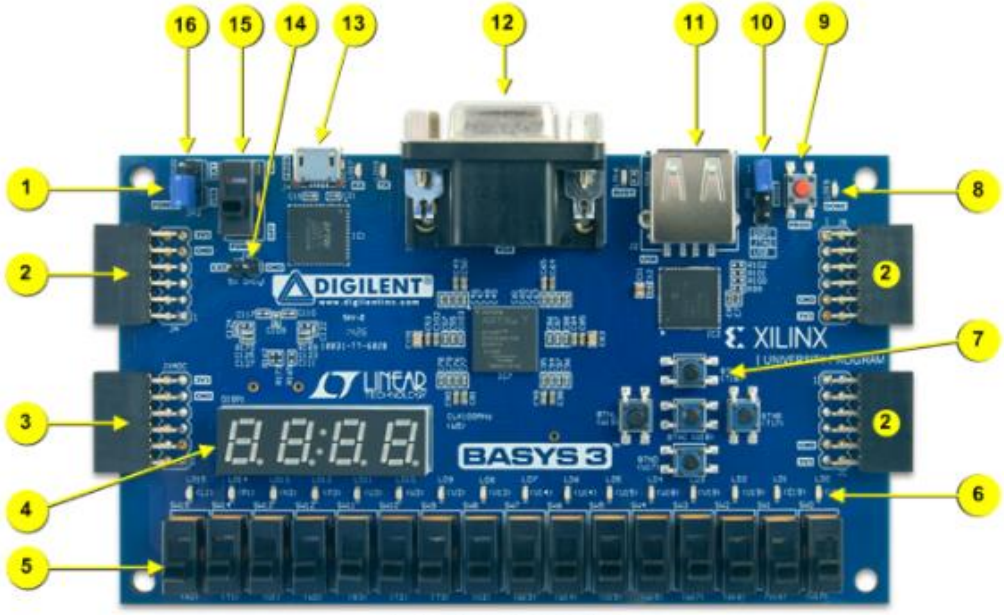
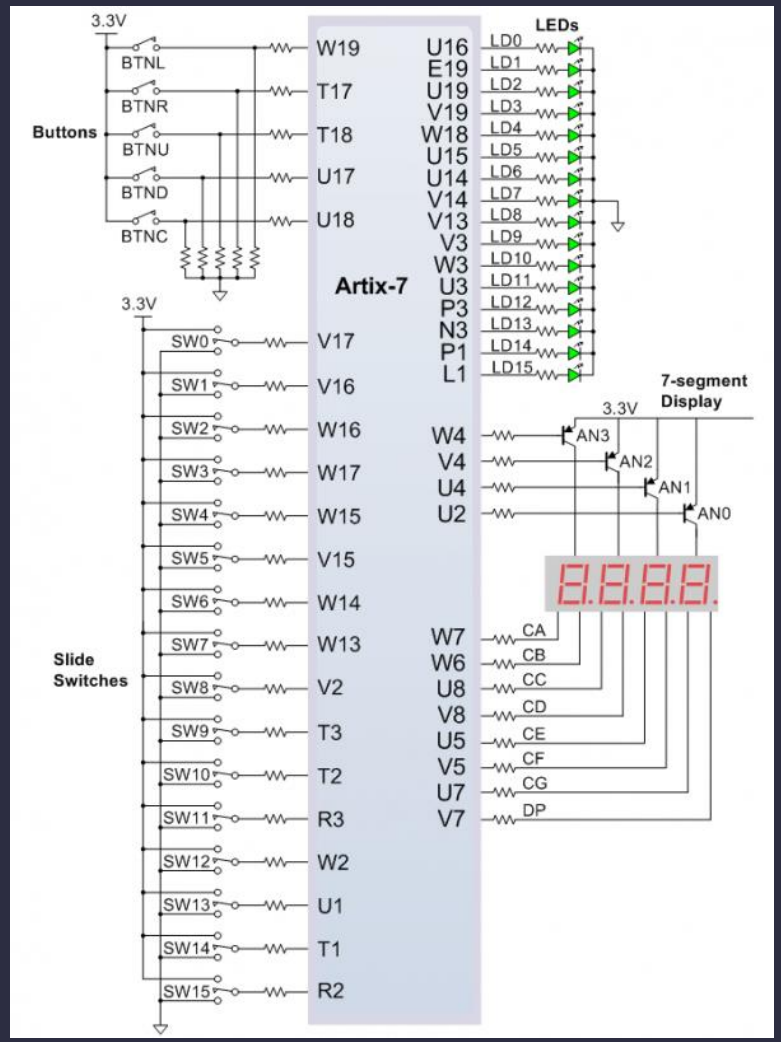


Figure 1. Basys3 board features

Callout	Component Description	Callout	Component Description
1	Power good LED	9	FPGA configuration reset button
2	Pmod connector(s)	10	Programming mode jumper
3	Analog signal Pmod connector (XADC)	11	USB host connector
4	Four digit 7-segment display	12	VGA connector
5	Slide switches (16)	13	Shared UART/ JTAG USB port
6	LEDs (16)	14	External power connector
7	Pushbuttons (5)	15	Power Switch
8	FPGA programming done LED	16	Power Select Jumper

Verilog – Combinational Circuits



Verilog – Combinational Circuits

Constraint (XDC) File

http://levent.tc/files/courses/digital_design/labs/basys3.xdc