Digital Design

Week 4: Sequential Circuits Part I



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Course



- Sequential Circuits
 - In sequential circuit, the output depends not only on the current inputs, but also on previous inputs.
 - Example: Counter counting up with a summation circuit

Memory storage unit called flip-flop







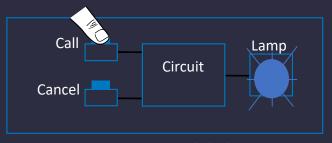
- Flight attendant call button
 - When pressed, the lamp remains active until it is pressed again.
 - When pressed again, the lamp turns off

combinatorial circuits?

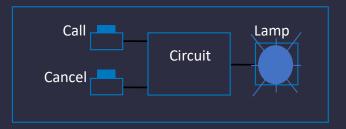


It will not work because the lamp will only be 1 when the call is pressed. The lamp will turn to 0 when the call button is not pressed. A register that holds the previous state of the circuit is needed for the desired behavior

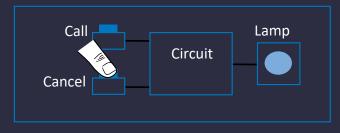




1. Button pressed, light on

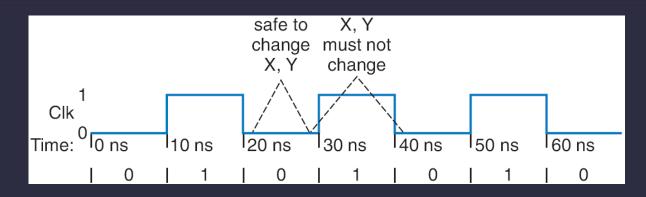


2. The button is released, the light remains on



3. Canceled, light off



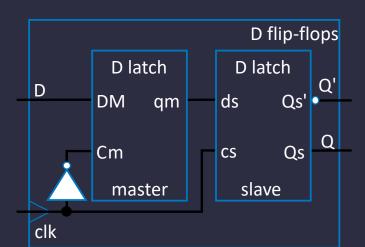


- *Clock Period*: The time between two rising edges
 - Period of the above signal: 20 ns
- Clock cycle:
 - Number of rising edge
- Clock Frequency: 1/ period
 - The period of the above signal = 1/20 ns = 50 MHZ

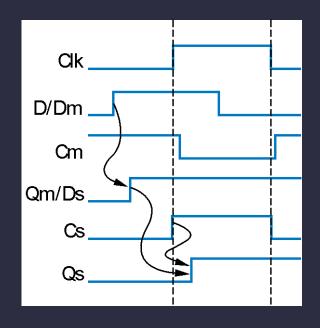
Freq	Period
100GHz	0.01 ns
10GHz	0.1 ns
1GHz	1 ns
100MHz	10 ns
10MHz	100 ns



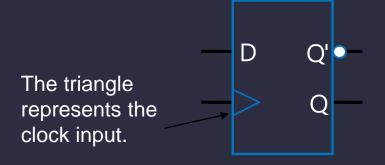
- *Flip-flop*: Samples the signal coming from outside on the rising edge of the incoming clock
- Design example master slave
 - 2 D latch is used.





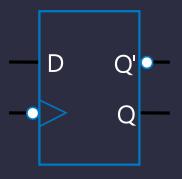






Rising Edge active flip flop notation



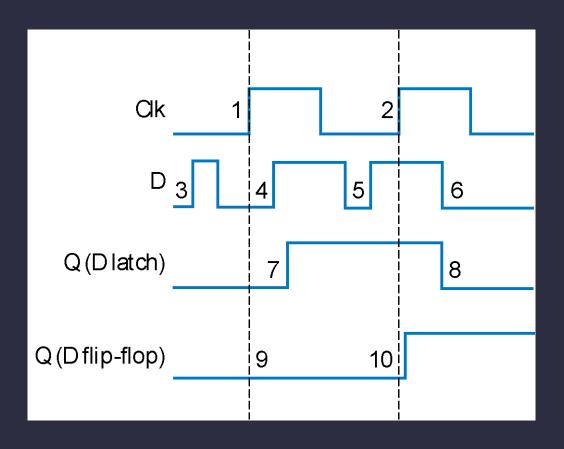


Falling Edge active flip flop notation



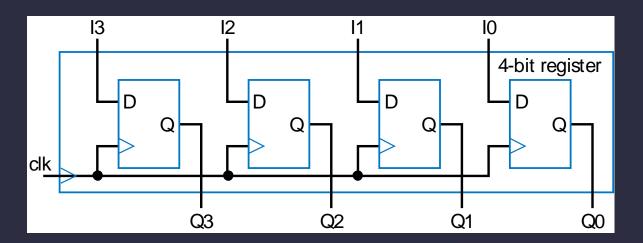


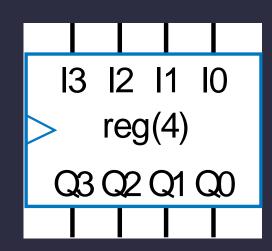
- D latch
- D -flip flop





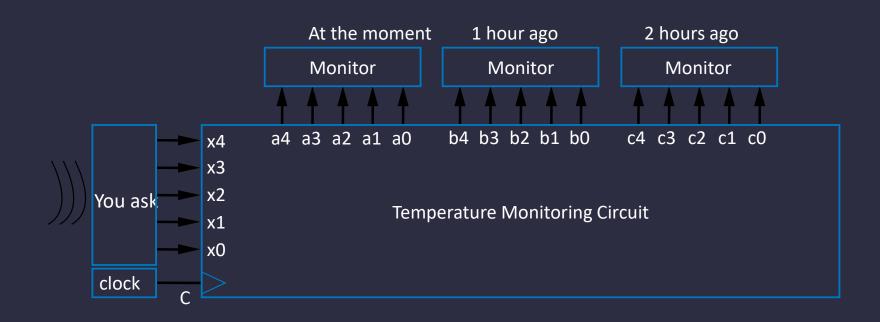
- When multiple bits need to be held, D flip flops are used together.
 - For example, when a 4-bit number needs to be kept
- Multi flip *Register* to the structure where the flops are held together *it is called*.







- Temperature Circuit
 - Temperature sensor gives a 5 bit output.
 - Clock's period is 1 hour. (It's a pretty slow clock)
 - Each clock on the rising edge and displays it to the monitor.





• 5bit registers

