Digital Design

Week 4: Sequential Logic Part II



Fenerbahce University



Course

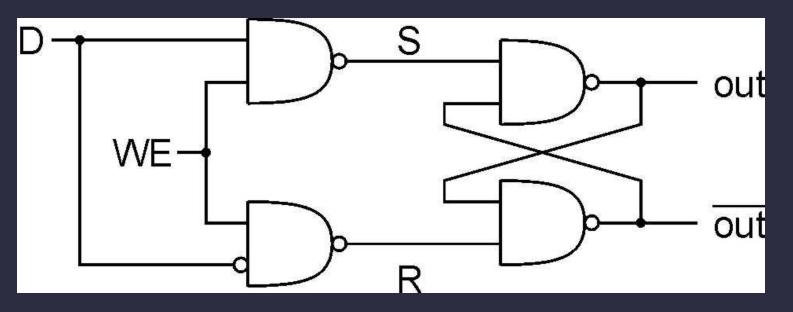
- Sequential Circuits
 - Clock Crystal
 - Clock Cycle
 - Type D Storages



D Type Holders (D Latch)

• It has two entrances. These; D (data) and WE (Write Access)

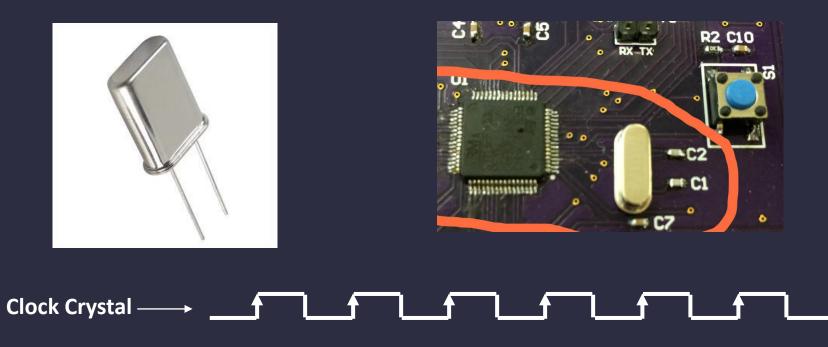
- WE = 1 encloses the value at input D.
 - S = NOT(D), R = D
- WE = 0 keeps its previous value.





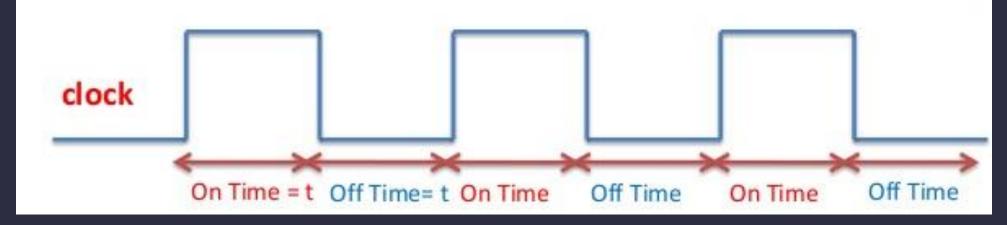
Clock Crystal

- It periodically generates a square-type signal.
- It's like someone is turning a switch on and off at regular intervals...





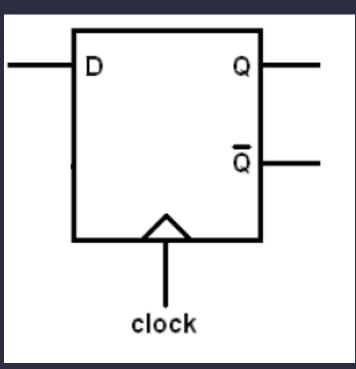
Clock



- Clock signal given in the figure repeats itself in 2t time/period.
- Each period of clock called clock cycle.
- It means Frequency = 1/Period.

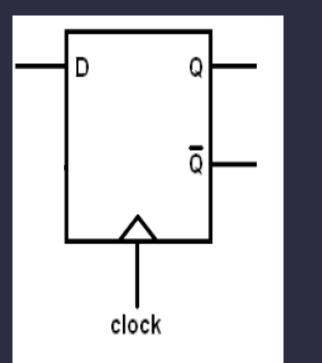


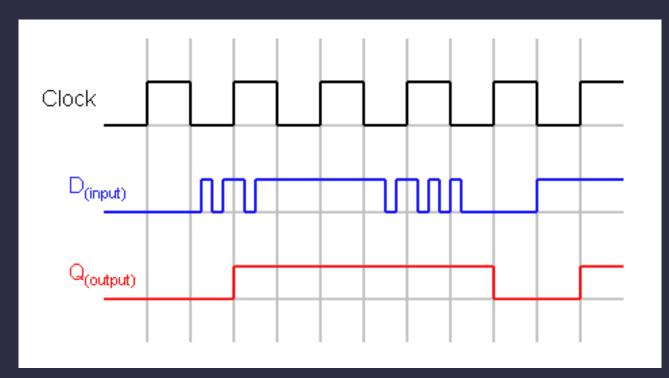
- When the rising or falling edge of the clock signal comes to itself, it transfers the value at the D input to the Q output.
- In other cases, the value at output Q does not change, even if input D changes.





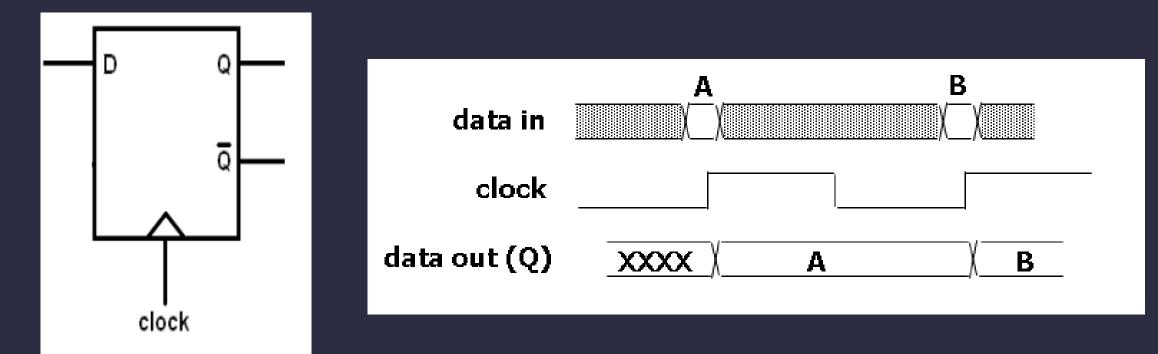
• Rising edge D-Type Storage Inputs and Outputs



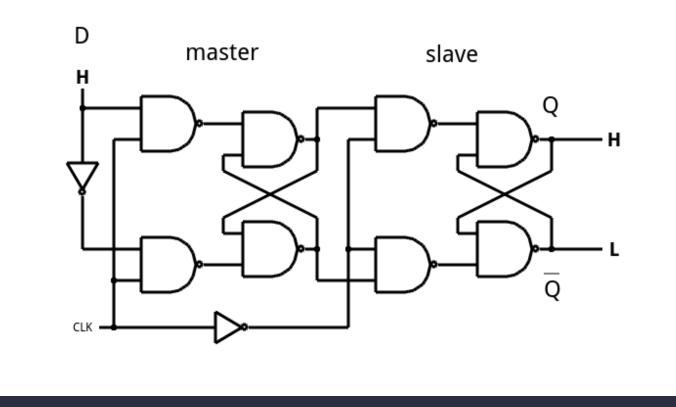




• Rising edge D-Type Storage Inputs and Outputs



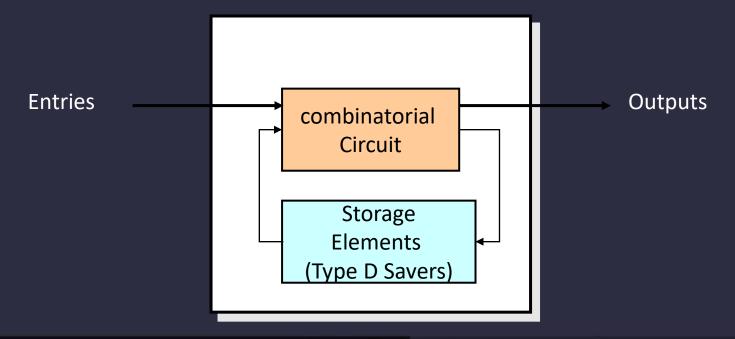




D Type Storage

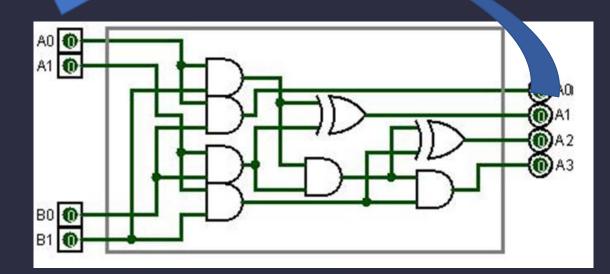


- Combinational circuits and storage elements.
- With the use of storage elements, the previous values produced by the circuit can also be used.



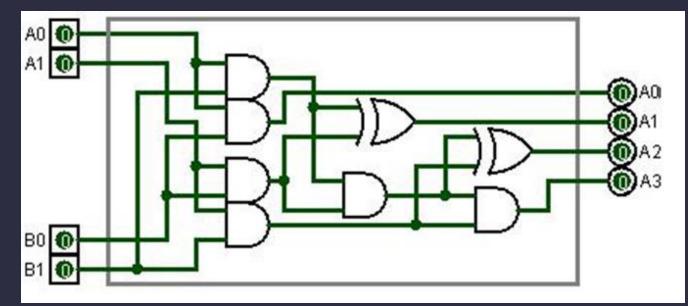


- When is it necessary?
- If the result produced by a circuit will be fed as an input to the circuit;



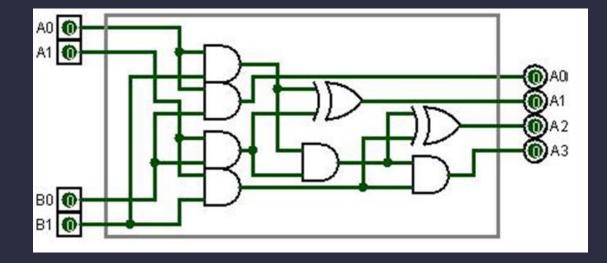


- When is it necessary?
- In order for the circuit to produce correct results, all inputs must remain constant.



• When is it necessary?

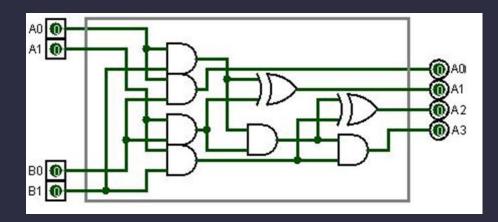
• Each output in this example comes from different logic gate paths.



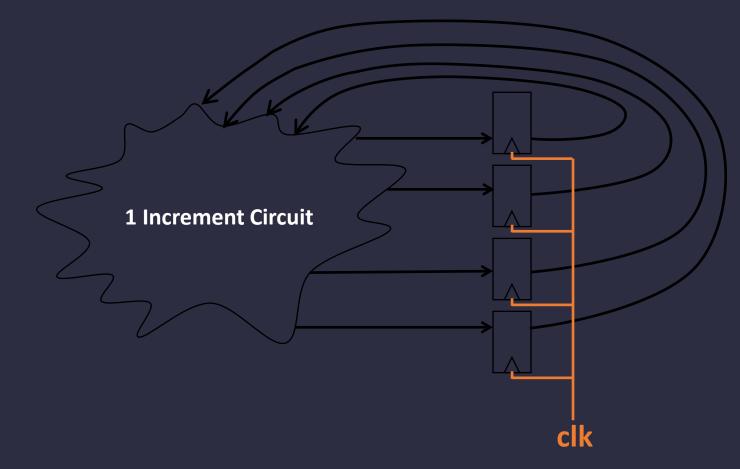




- When is it necessary?
- Therefore, when we connect the output signals directly to the input, the input is changed before the circuit correct output values.
- Correct results can never be captured.





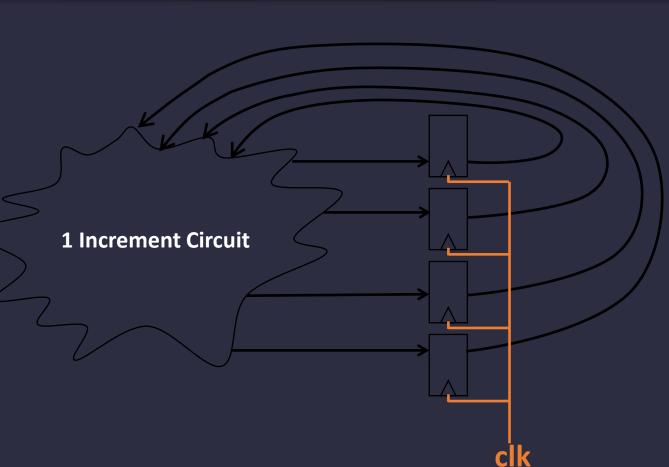


4 Bit 1 increment circuit.

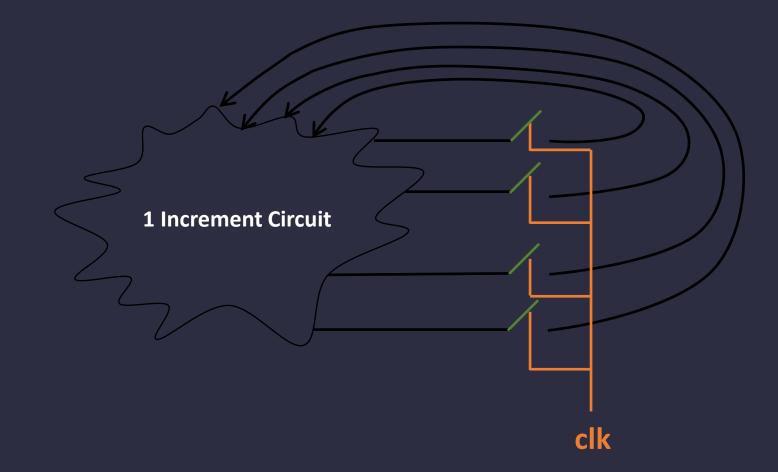


Clock input is as much as the slowest output produced by the circuit

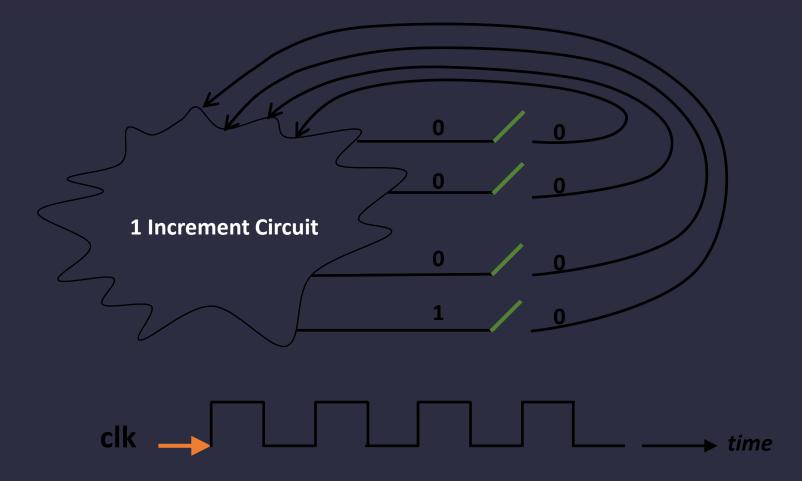
All outputs of the circuit will be fed back to the circuit by waiting until the slowest output output.



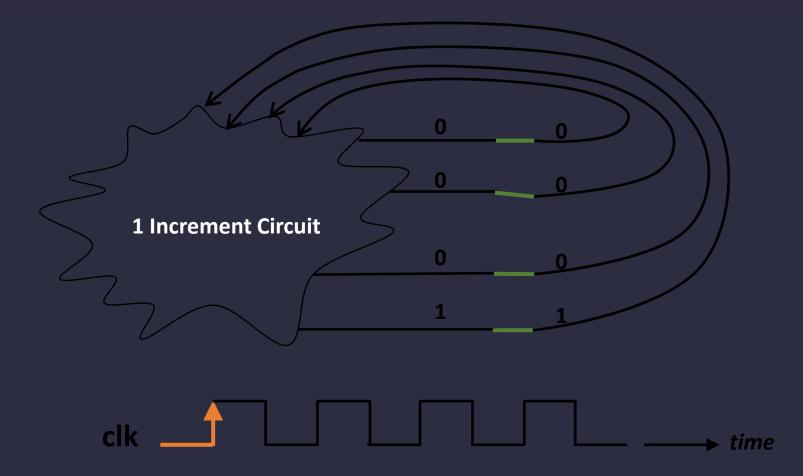




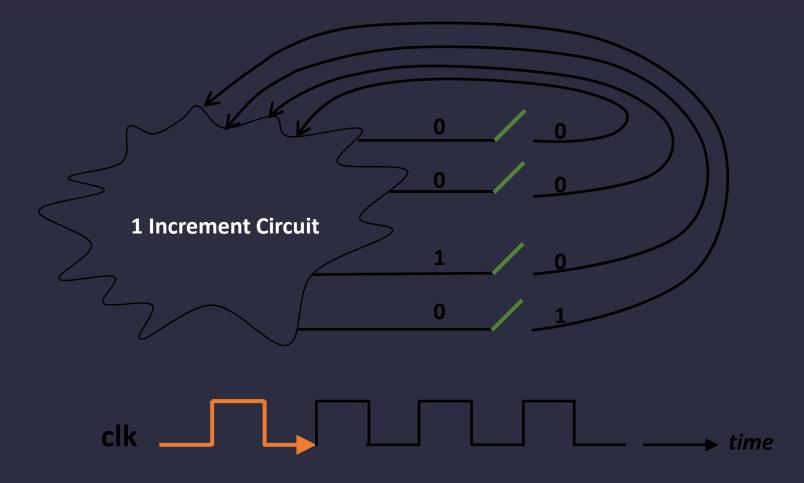




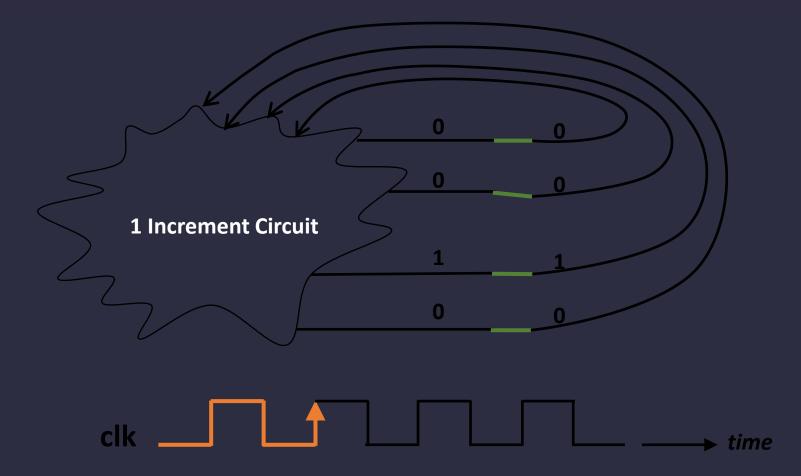




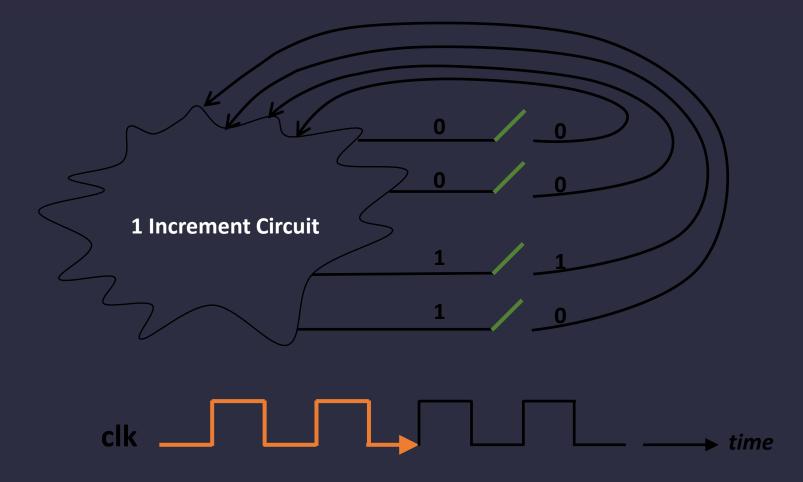




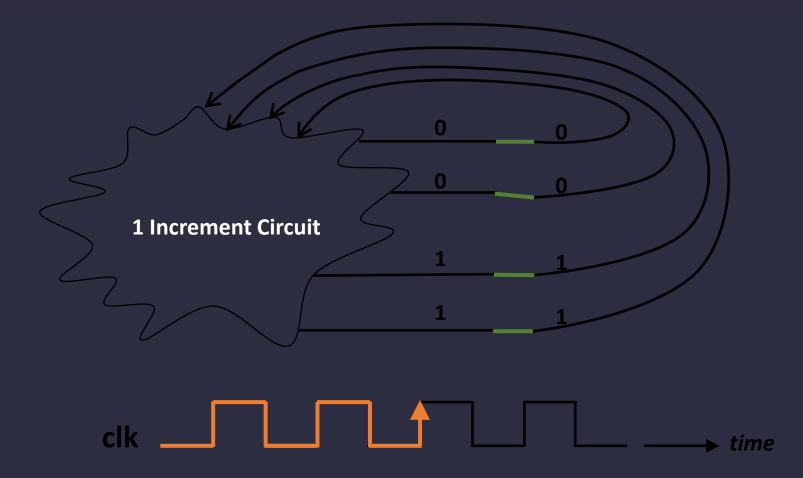




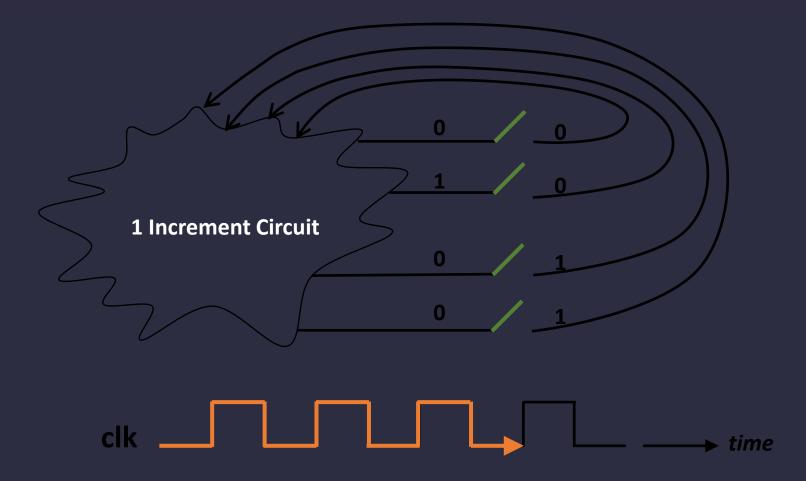




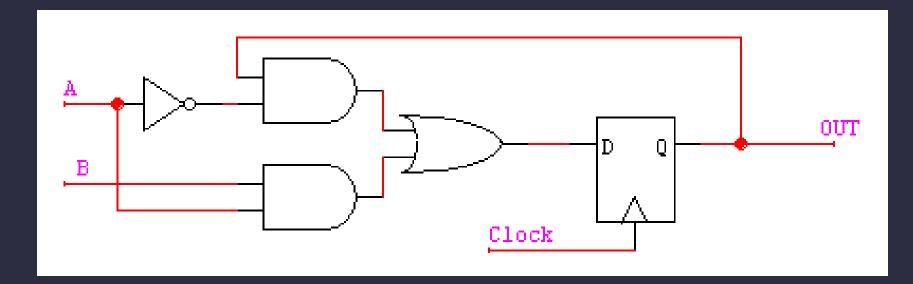












Combinational Circuit and Sequential Circuit with Register