

Mantıksal Sistem Tasarımı – BLM 201

Hafta 6: Durum Makinaları Bölüm II

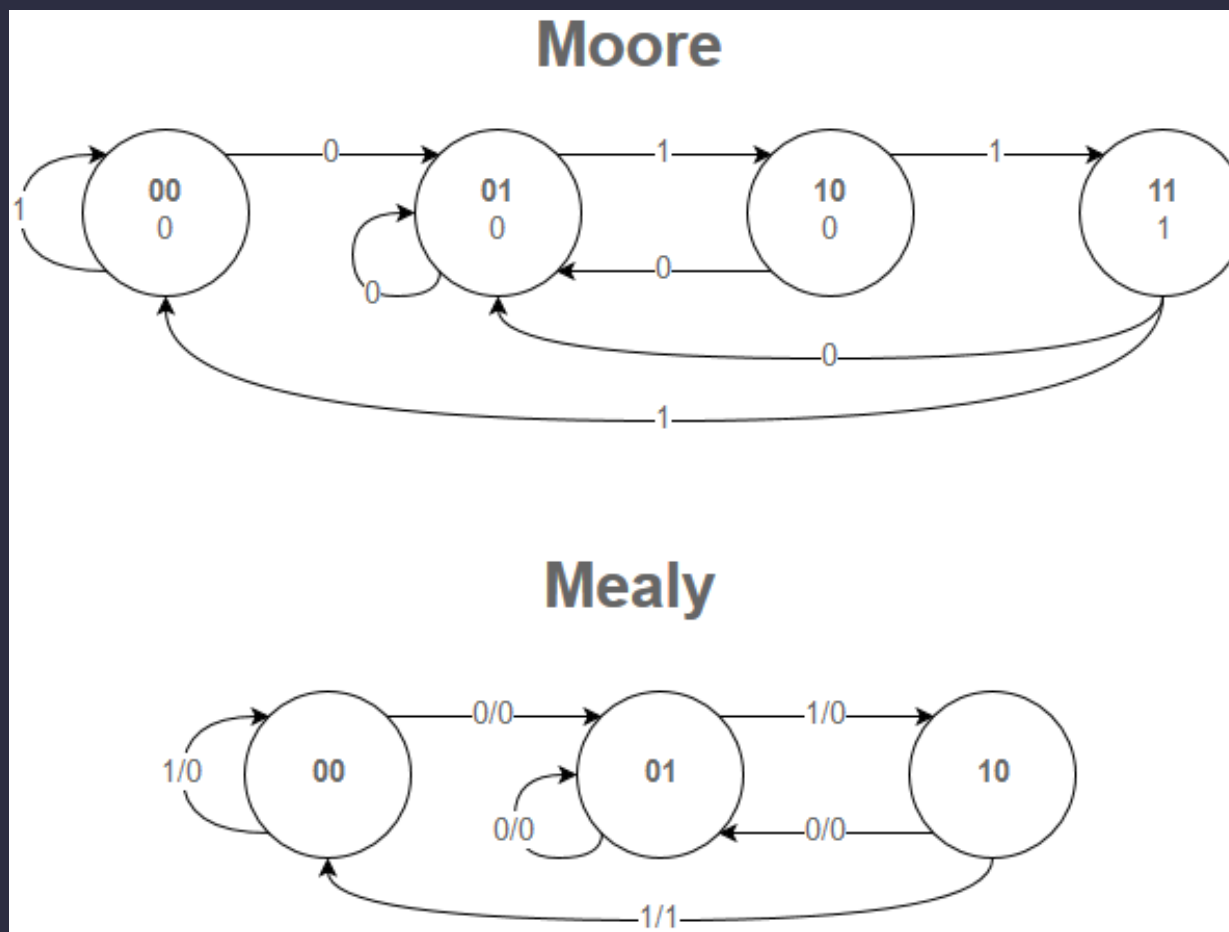


Fenerbahçe Üniversitesi

5. Hafta İçeriği

- Durum Makinaları
 - Durum Makinaları Verilog Gösterimleri

Durum Makinaları



Moore Durum Makinası Örnekleri

Durum Makinaları

```
module stateMachineTest (input clk, input in, output reg out)
```

```
  reg [1:0] state, stateNext;  
  reg outNext;
```

```
  initial begin
```

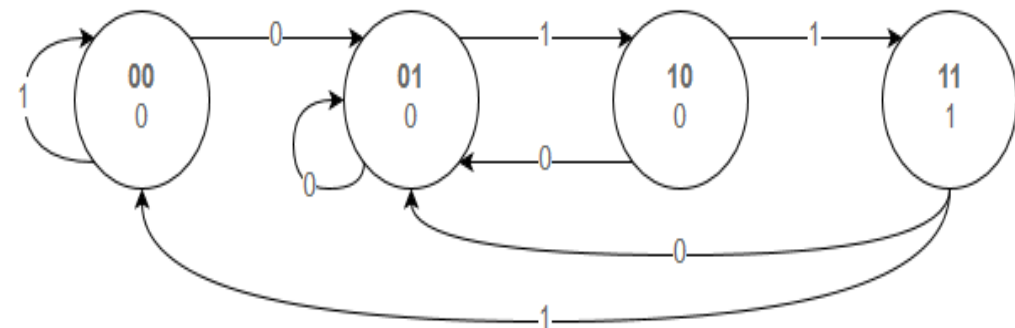
```
    state = 0;  
    stateNext = 0;  
    out = 0;  
    outNext = 0;
```

```
  end
```

```
  always@(posedge clk) begin  
    state <= stateNext;  
    out <= outNext;
```

```
  end
```

Moore



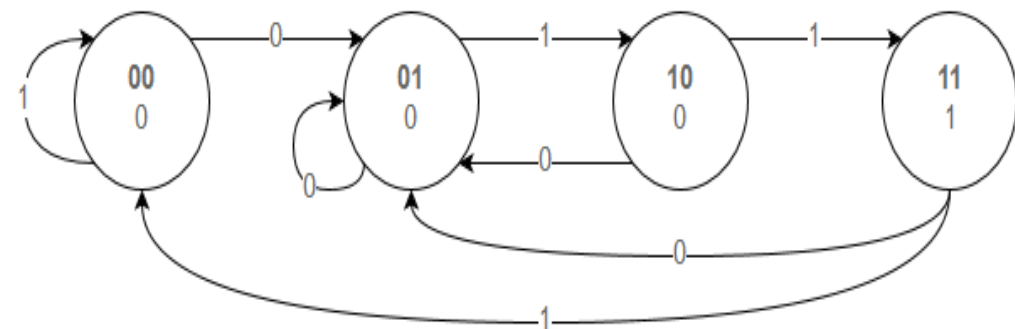
Durum Makinaları

```

always@(*) begin
    stateNext = state;
    outNext = out;
    case(state)
        0: begin
            if(in == 0)begin
                stateNext = 1;
                outNext = 0;
            end
        end
    endcase
end
endmodule

```

Moore



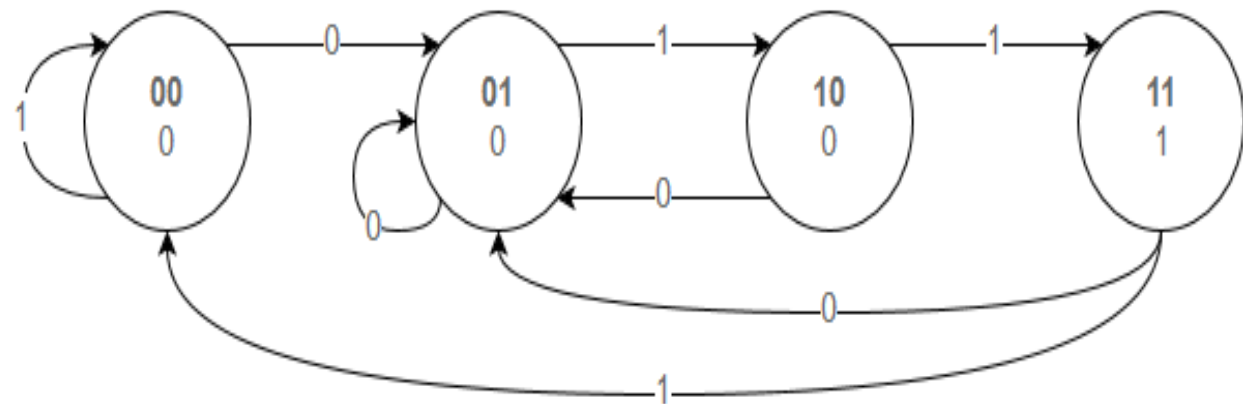
Durum Makinaları

```

1: begin
    if(in == 1)begin
        stateNext = 2;
        outNext = 0;
    end
end
2: begin
    if(in == 1)begin
        stateNext = 3;
        outNext = 1;
    end else begin
        stateNext = 1;
        outNext = 0;
    end
end
3: begin
    if(in == 0)begin
        stateNext = 1;
        outNext = 0;
    end else begin
        stateNext = 0;
        outNext = 0;
    end
end
end

```

Moore



Durum Makinaları

```
module mooreMachine2 (input clk, input ResetN, input w, output reg z)
```

```
  reg [1:0] state, stateNext;
  reg zNext;
```

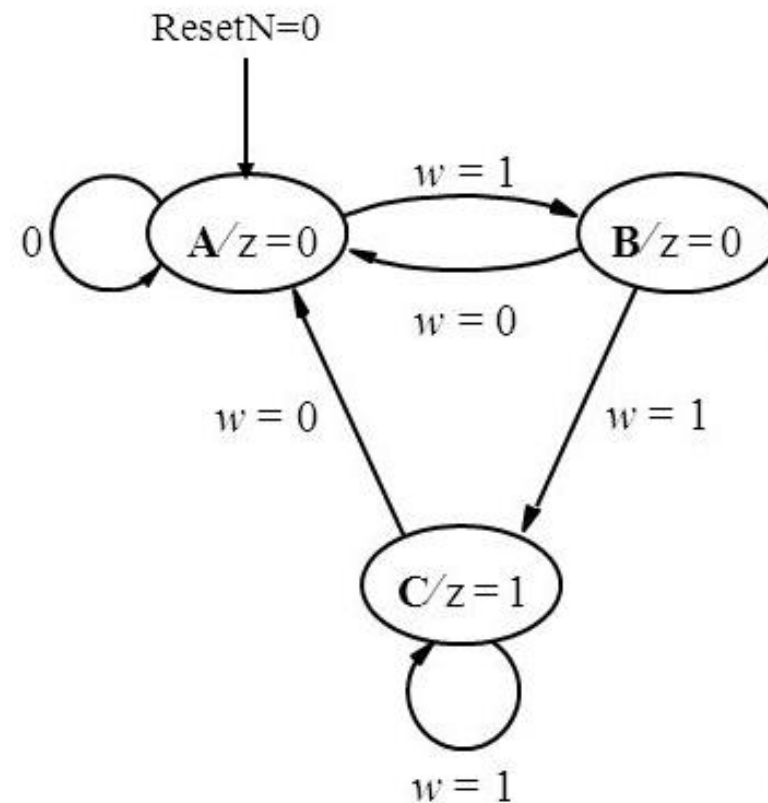
```
  initial begin
```

```
    state = 0;
    stateNext = 0;
    z = 0;
    zNext = 0;
```

```
  end
```

```
  always@(posedge clk) begin
    state <= stateNext;
    z <= zNext;
```

```
  end
```

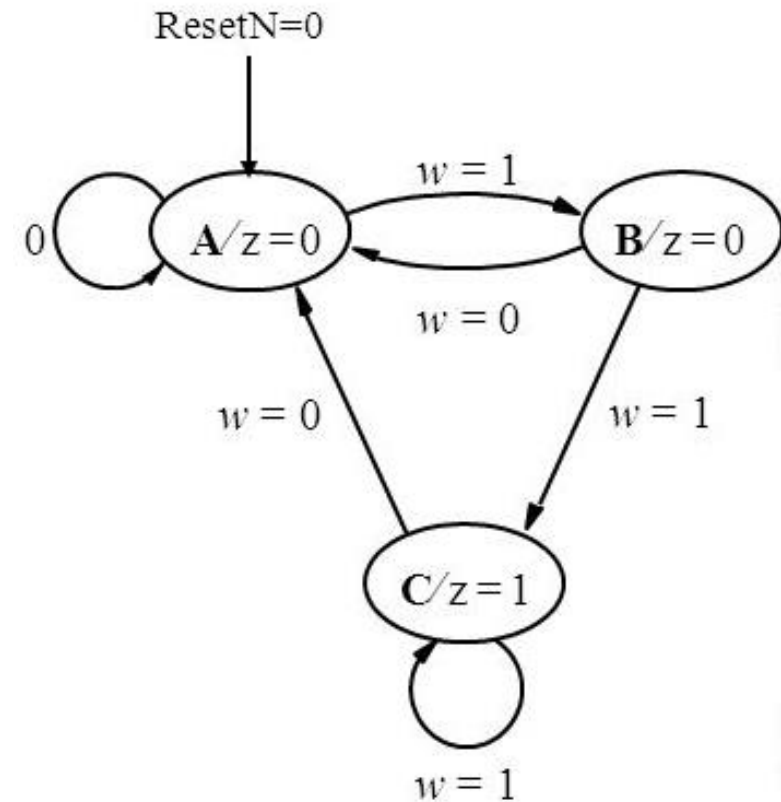


Durum Makinaları

```

always@(*) begin
    stateNext = state;
    zNext = z;
    if(ResetN) begin
        stateNext = 0;
        zNext = 0;
    end else begin
        case(state)
            0: begin
                if(w == 1)begin
                    stateNext = 1;
                    zNext = 0;
                end
            end
        endcase
    end
end
endmodule

```

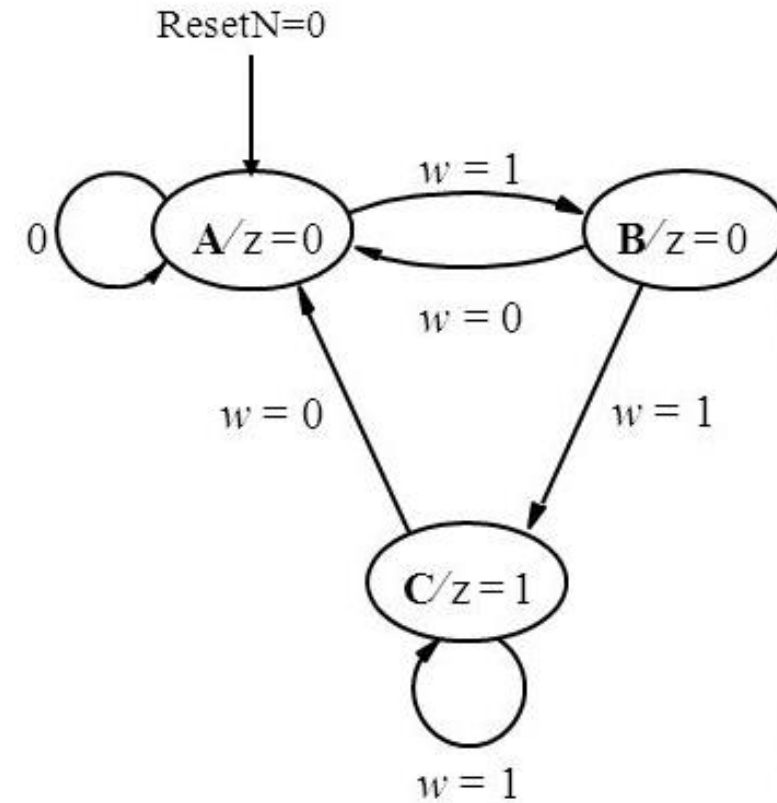


Durum Makinaları

```

1: begin
  if(w == 0)begin
    stateNext = 0;
    zNext = 0;
  end else begin
    stateNext = 2;
    zNext = 1;
  end
end
2: begin
  if(w == 0)begin
    stateNext = 0;
    zNext = 0;
  end
end
end

```



Mealy Durum Makinası Örnekleri

Durum Makinaları

```
module mooreMachine1 (input clk, input in, output reg out)
```

```
reg [1:0] state, stateNext;
```

```
initial begin
```

```
    state = 0;
```

```
    stateNext = 0;
```

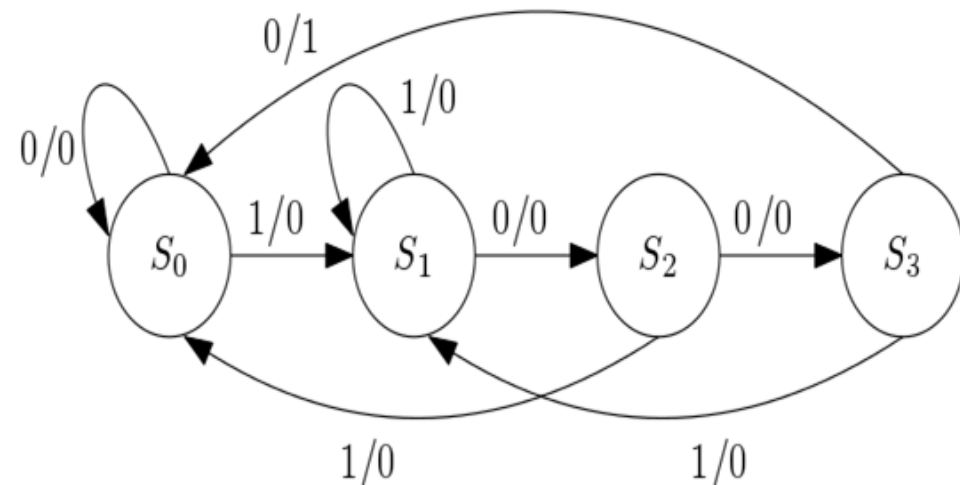
```
    out = 0;
```

```
end
```

```
always@(posedge clk) begin
```

```
    state <= stateNext;
```

```
end
```

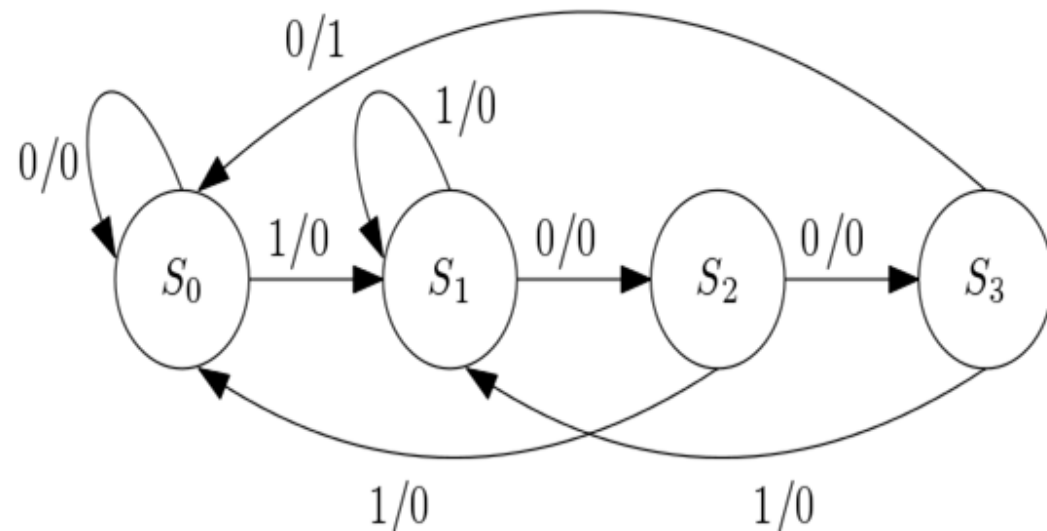


Durum Makinaları

```

always@(*) begin
  stateNext = state;
  out = 0;
  case(state)
    0: begin
      if(in == 0)begin
        out = 0;
      end else begin
        out = 1;
        stateNext = 1;
      end
    end
  endcase
end

```

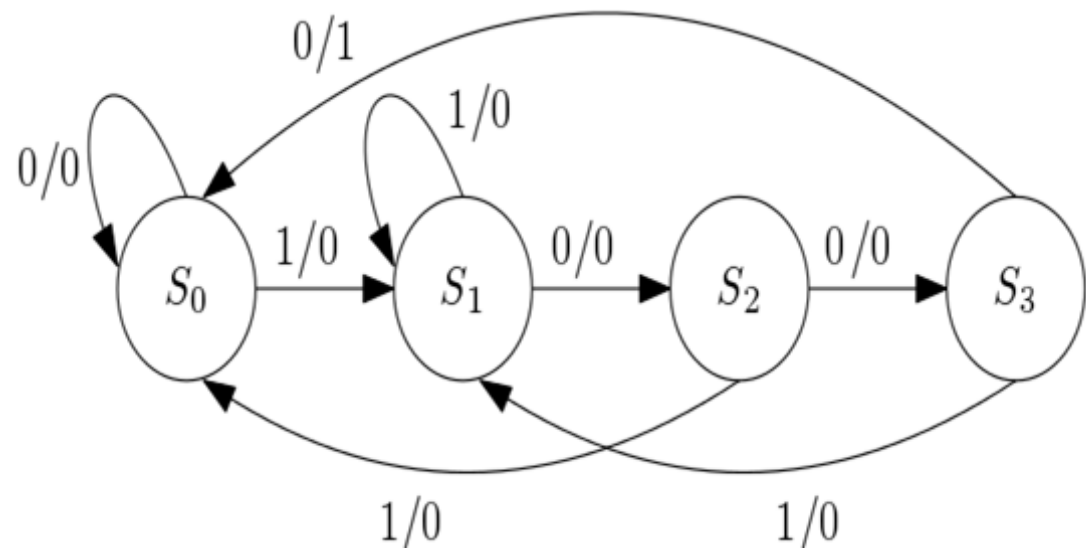


Durum Makinaları

```

1: begin
    if(in == 0)begin
        out = 0;
        stateNext = 2;
    end else begin
        out = 0;
    end
end
2: begin
    if(in == 0)begin
        out = 0;
        stateNext = 3;
    end else begin
        out = 0;
        stateNext = 0;
    end
end
3: begin
    if(in == 0)begin
        out = 1;
        stateNext = 0;
    end else begin
        out = 0;
        stateNext = 1;
    end
end
end

```



Durum Makinaları

```
module mooreMachine2 (input clk, input in, output reg out)
```

```
reg [1:0] state, stateNext;
```

```
initial begin
```

```
    state = 0;
```

```
    stateNext = 0;
```

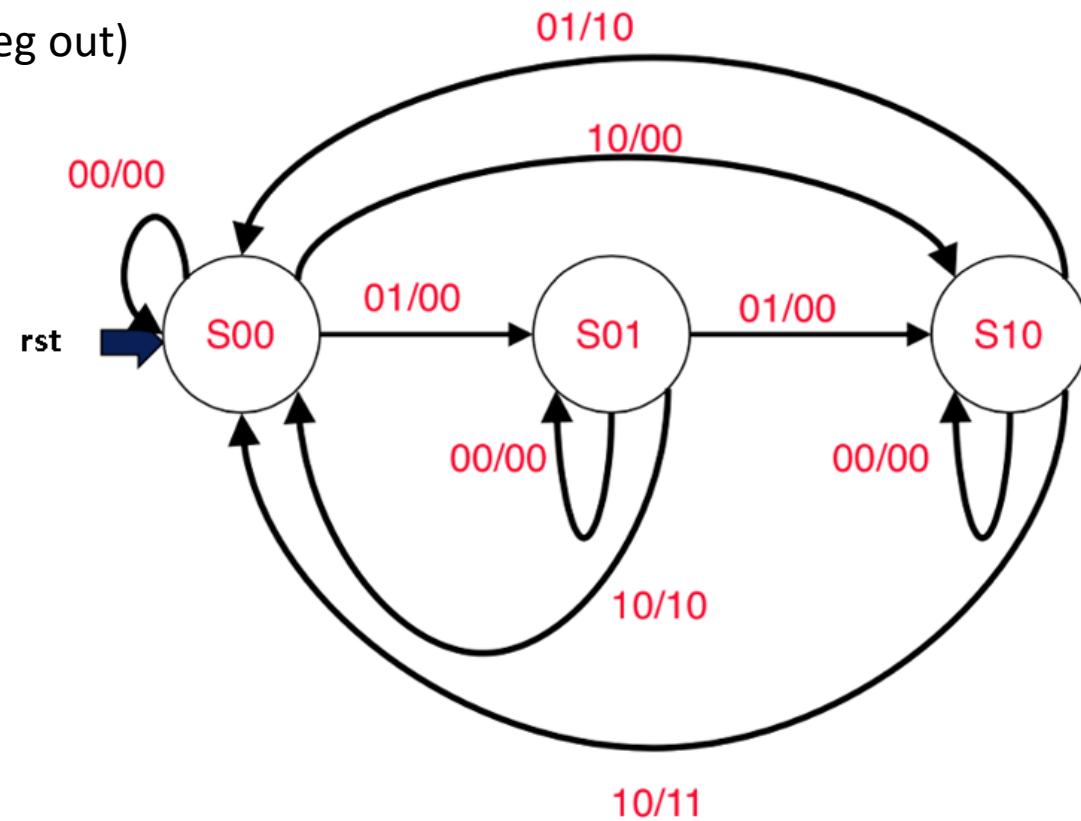
```
    out = 0;
```

```
end
```

```
always@(posedge clk) begin
```

```
    state <= stateNext;
```

```
end
```

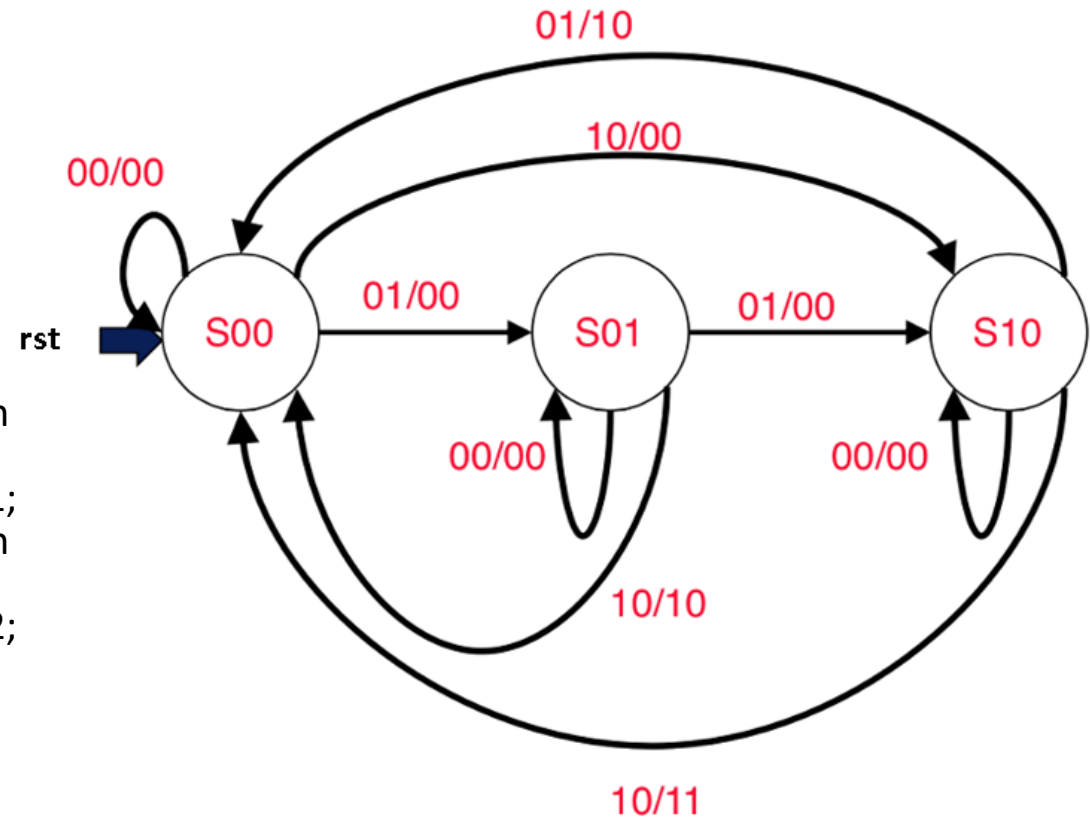


Durum Makinaları

```

always@(*) begin
    stateNext = state;
    out = 0;
    if(rst) begin
        stateNext = 0;
        out = 0;
    end else begin
        case(state)
            0: begin
                if(in == 0)begin
                    out = 0;
                end else if(in == 1) begin
                    out = 0;
                    stateNext = 1;
                end else if(in == 2) begin
                    out = 0;
                    stateNext = 2;
                end
            end
        endcase
    end
end
end
endmodule

```



Durum Makinaları

```

1: begin
  if(in == 0)begin
    out = 0;
  end else if(in == 1) begin
    out = 0;
    stateNext = 2;
  end else if(in == 2) begin
    out = 2;
    stateNext = 2;
  end
end
end
2: begin
  if(in == 0)begin
    out = 0;
  end else if(in == 1) begin
    out = 2;
    stateNext = 0;
  end else if(in == 2) begin
    out = 3;
    stateNext = 0;
  end
end
end

```

