Digital Design

Week 11: Memories

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Couse plan

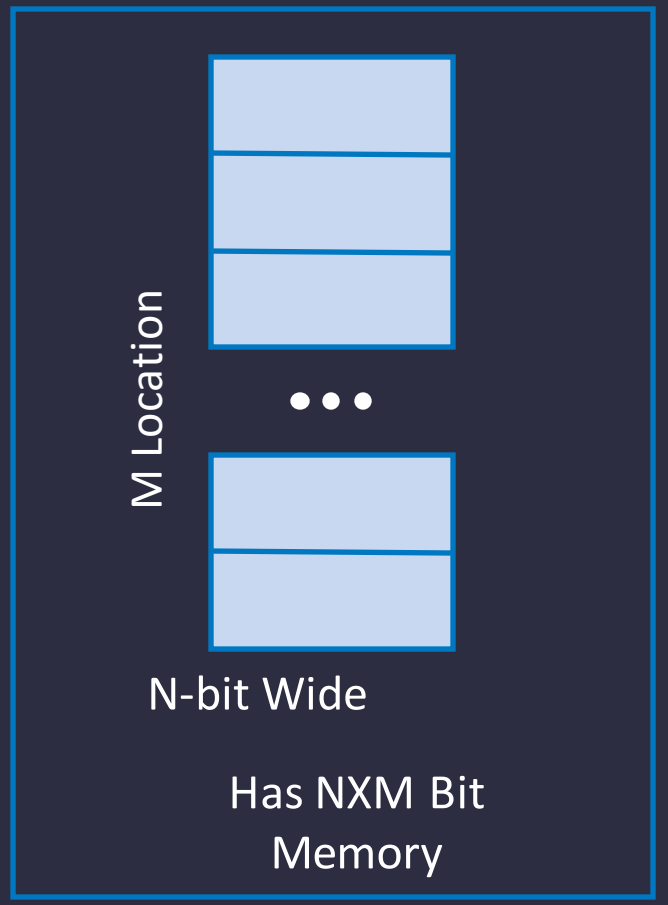
- Memory Elements
  - Random Access Memory
  - Read Only Memory
  - BRAM
  - DRAMA

Memory Elements

- A combinational circuit output can be stored in registers.
- However, the number of registers is quite limited.
- When the amount of data to be stored increases, instead of storing them in the register, we are using BRAM (Block RAM) or DRAM (Dynamic Random Access Memory).

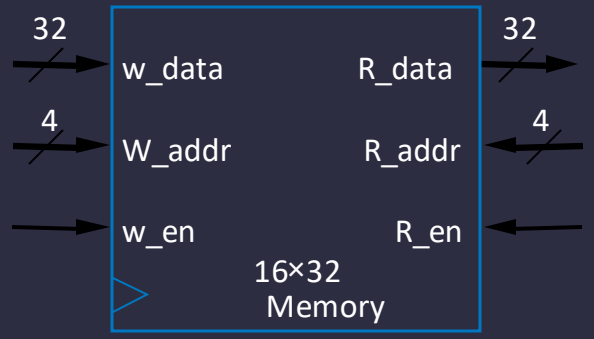
Memory Elements

- ***MxN Memory***
  - M locations , N bits wide



Random Access Memory (RAM)

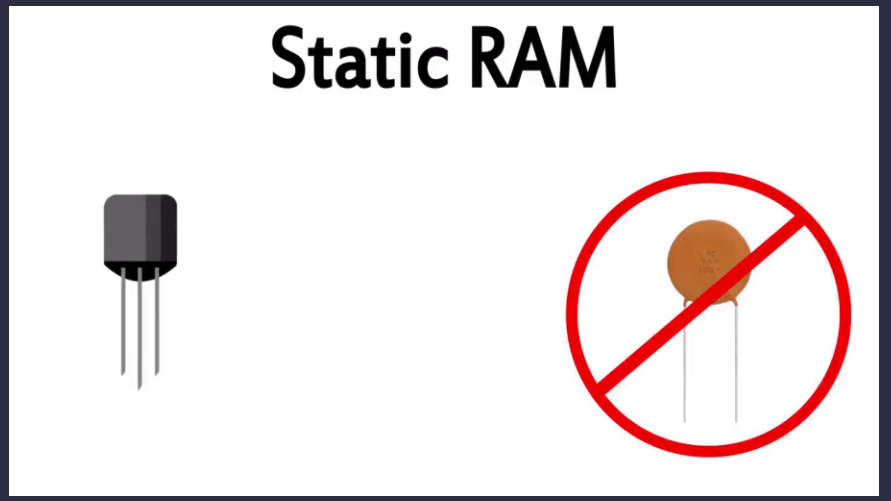
- RAM – It is both writable and readable memory.
  - Random Access Memory
    - This nomenclature is derived from the presence of tape type recording elements. There was only sequential access to such memories.
    - The feature of random access is that the desired address on the RAM can be accessed directly. In other words, it is not necessary to go through all previous addresses to go to an address in sequential access memories.
  - Memory can also be made with a group of registers.

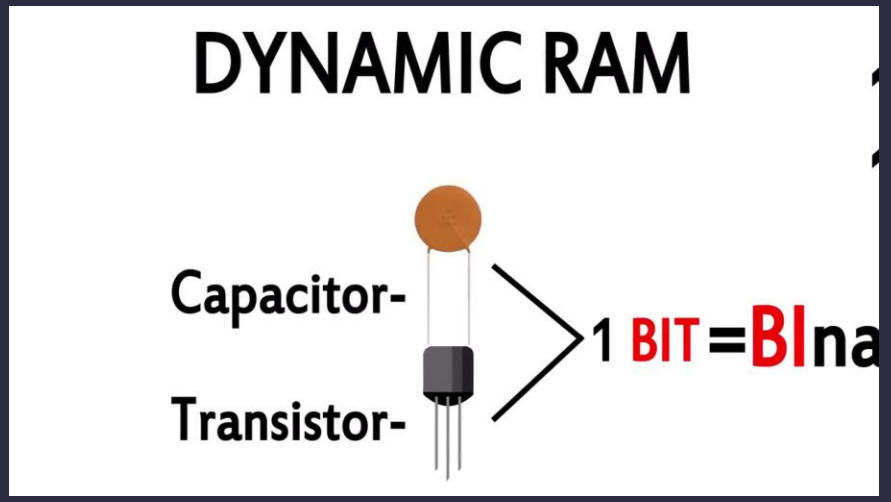


Random Access Memory (RAM)

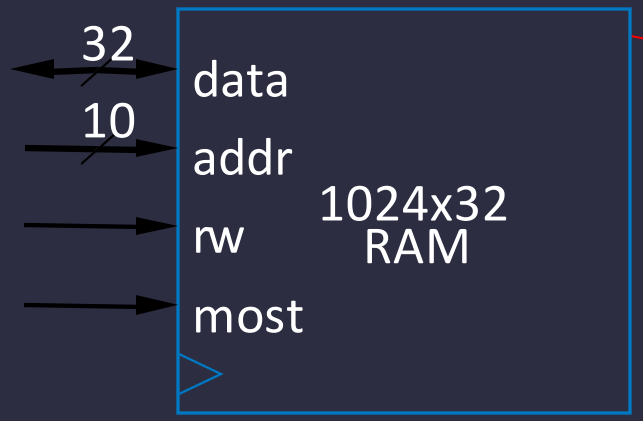
- RAMs can be divided into 2 groups

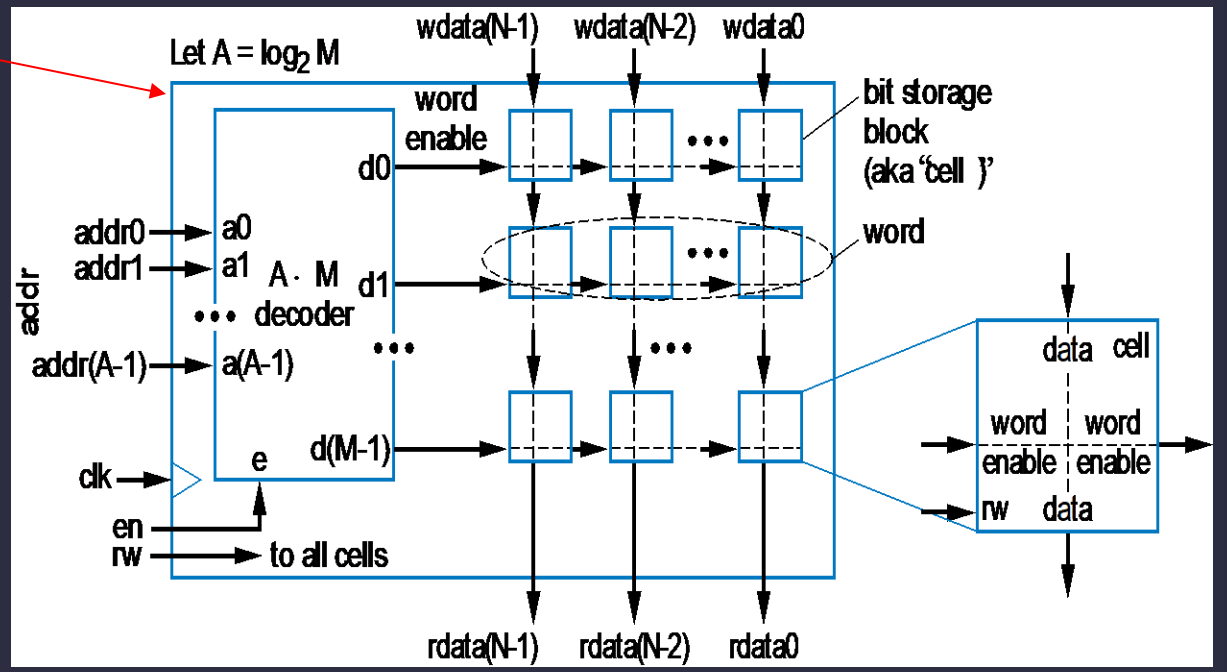
- Static
- Dynamic





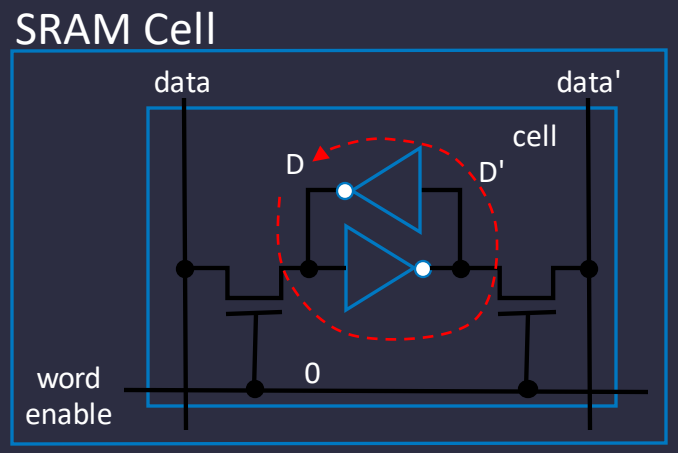
Static RAM (SRAM)

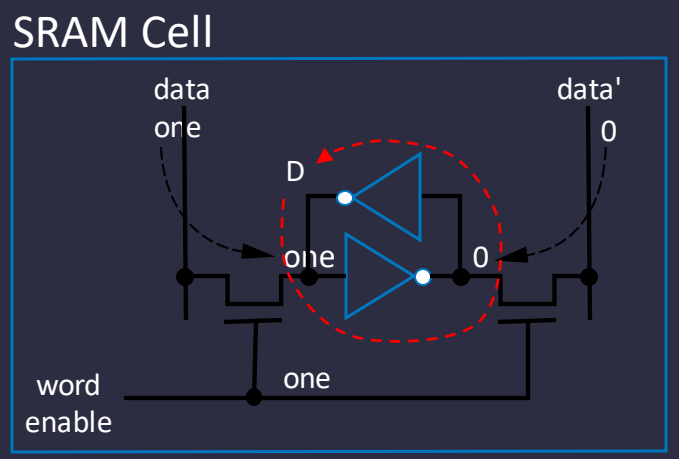


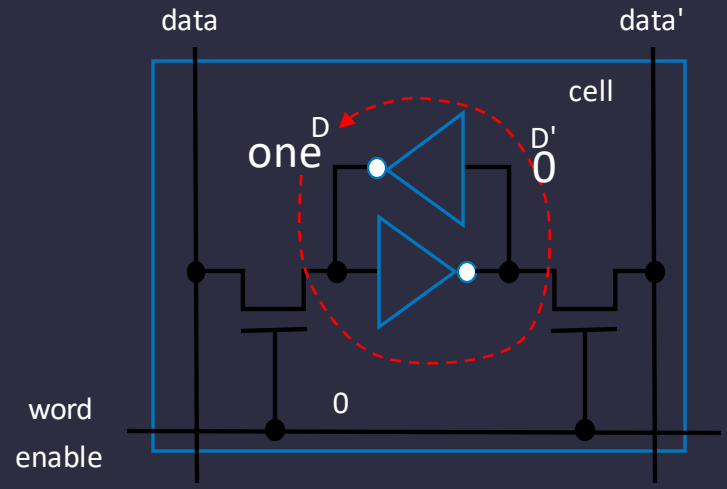


- Static Cell RAM
  - Consists of 6 transistors (Inverter uses 2 transistors)
  - Static RAMs is that they consist fully transistors .

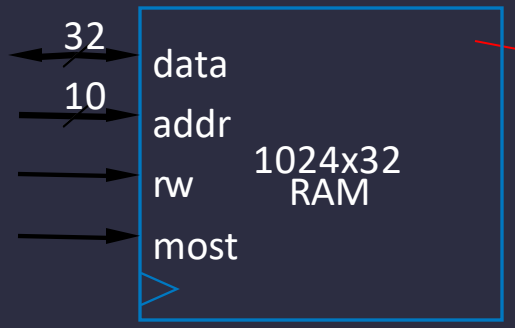
Static RAM (SRAM)

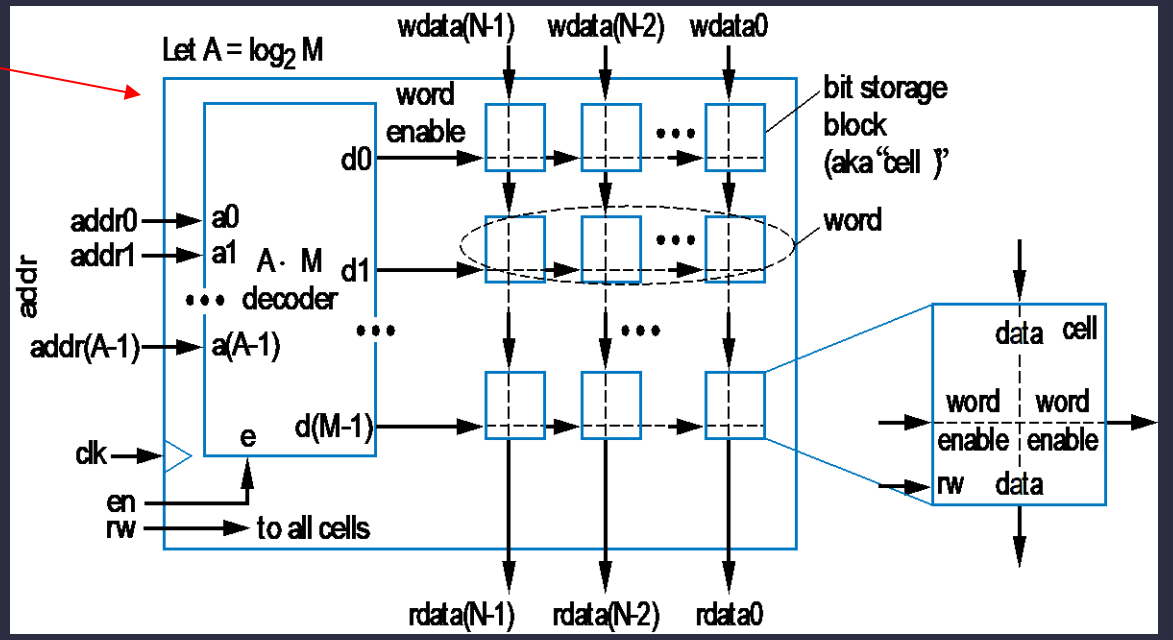






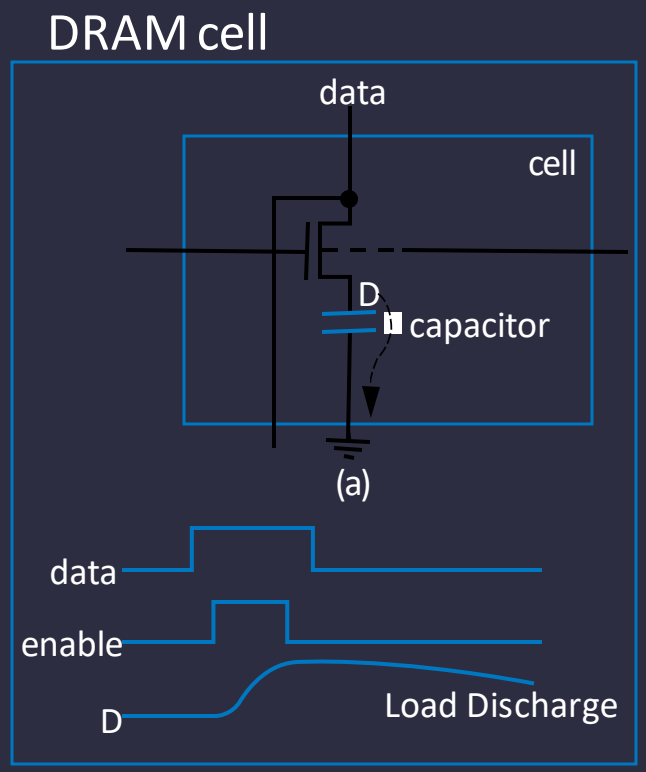
Dynamic RAM (DRAM)





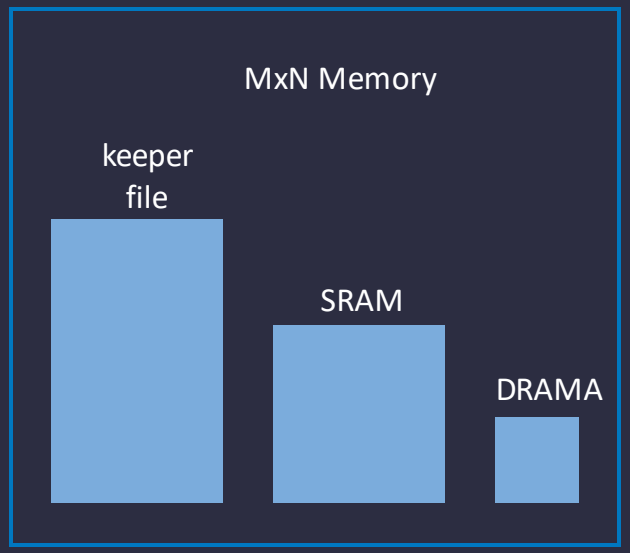
- Dynamic RAM Cell
  - 1 transistor
  - capacitor to store it.

Dynamic RAM (DRAM)



Memory Comparisons

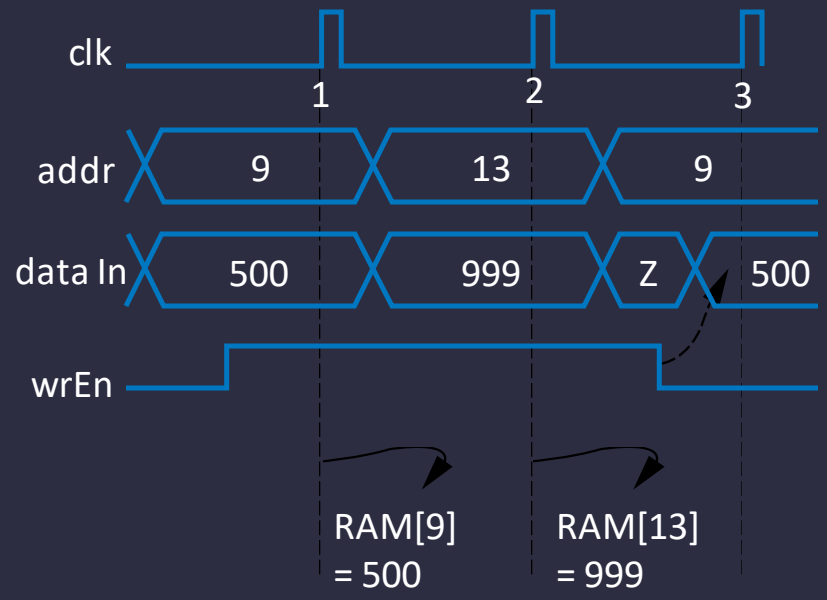
- Register File
  - Consists of registers
  - is the fastest
  - But it is the most expensive solution
  - The unit has the largest physical space as storage
- SRAM
  - It's fast
  - It is more compact than the storage.
  - in FPGAs BRAMs are SRAMs
- DRAM
  - It has the most access speed
    - Inaccessible during Refreshing times
  - However, it is the most compact structure compared to other memories.
  - DRAMs , if an address is to be accessed for the first time, it is accessed with a certain delay. There is no delay in the access of the addresses following this address.



Physical Space Occupied by Memory in Per Unit Area

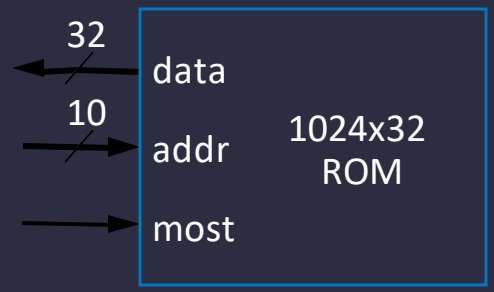
Writing and Reading

- Writing
  - *addr* Type the address where you want the RAM to be written to the port , however, pull the wrEn signal to 1 in parallel
- Read
  - *addr* by giving the address you want to be read to the port, 1 clock Read the data from the dataOut port after the cycle .



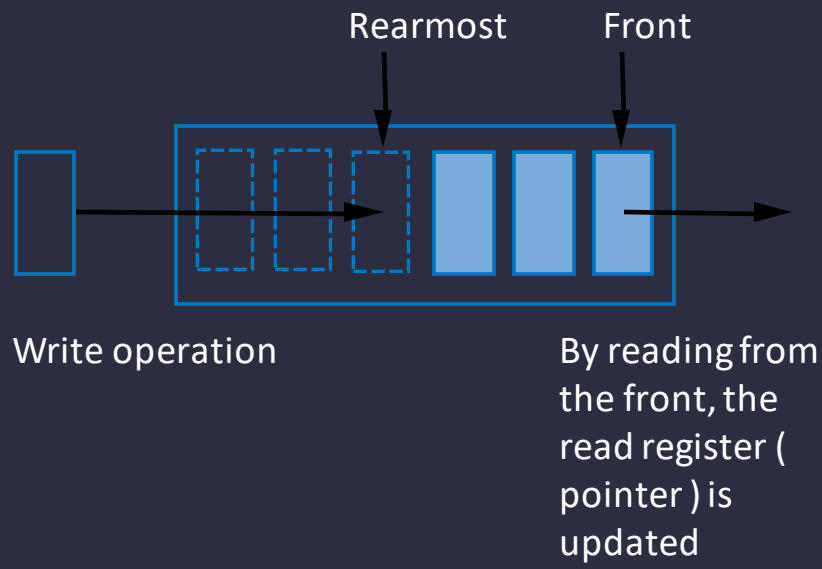
Read-Only Memory – ROM

- Only data can be read from such memories, not written.
  - There are only output ports
- Advantages over
  - This build is preferable if you want your memory to be non-replaceable.

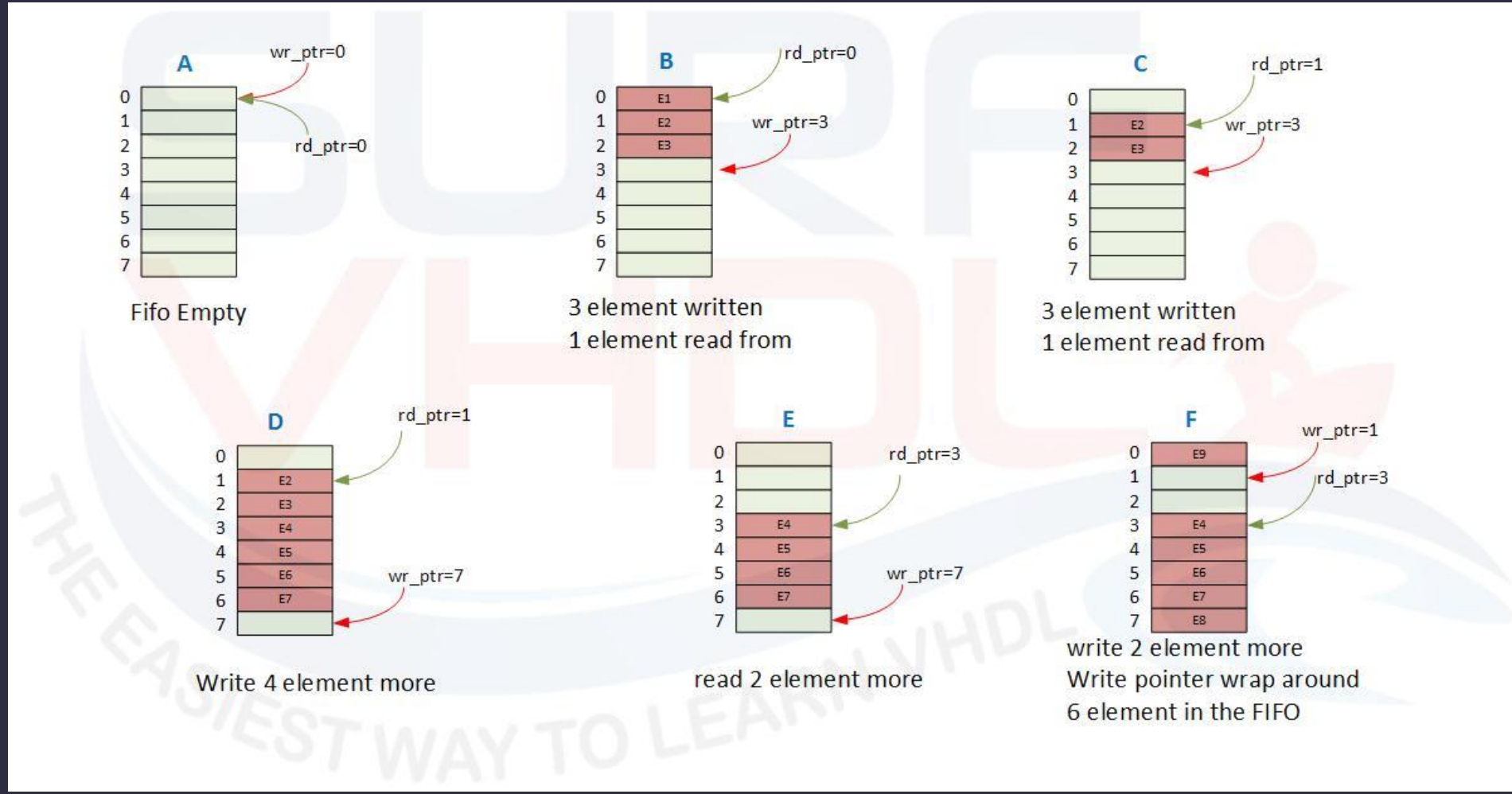


Queues – FIFO (First In First Out)

- *Queues are storage areas where first write is read first*
- push and pop.
- push operation is used to save the data to the storage area, and the pop operation is used to read the data from the field.



Queues – FIFO (First In First Out)



Queues – FIFO (First In First Out)

Examples:

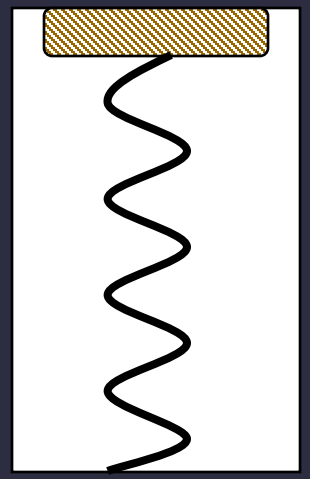
- Keyboard
  - keyboard fills keys pressed into a FIFO , the computer can read unless the FIFO is blank.
- Network routers _
  - incoming packets to a FIFO , then forwards it to the desired address, along with the

heaps

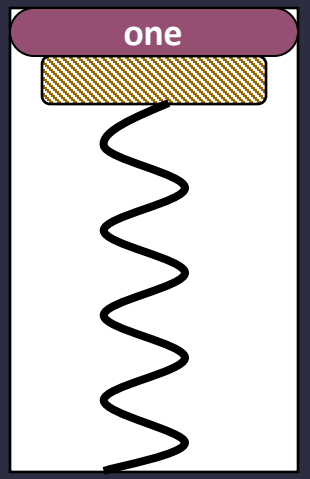
- LIFO (last-in first-out) is the storage structure .
  - The first data recorded, the last output .
  - If it's the last data saved on the stack, it's out first

- It has two main functions :
- PUSH: Adds data to the stack
- POP: Retrieves data from the stack

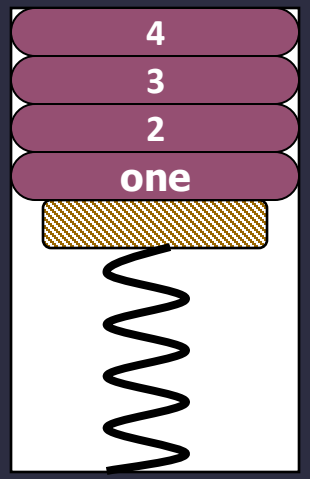
Stack Example



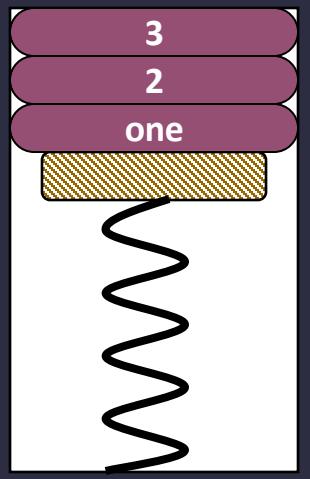
Initial Status



a data
after adding



3 more data
after adding



a data
when taken

Software Implementation

- The data does not move, the start address of the stack changes