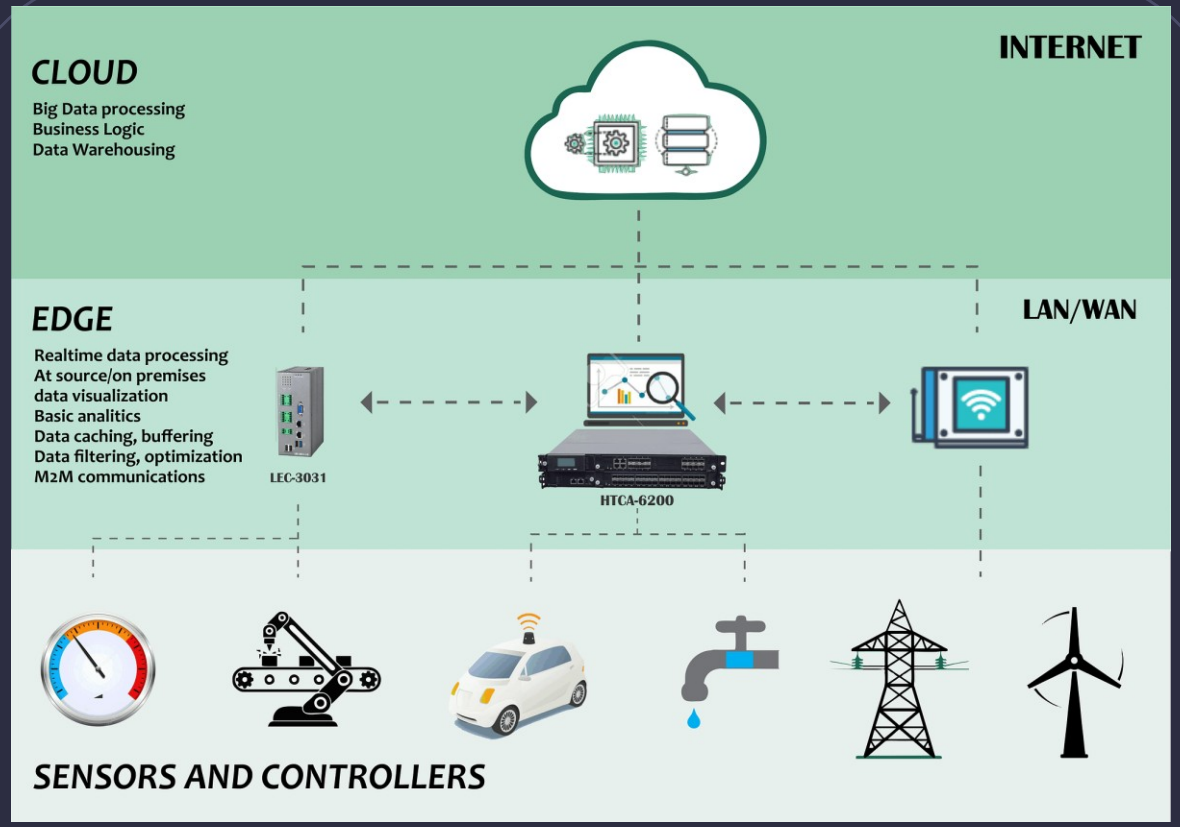
Internet of Things

Week 2: MCU

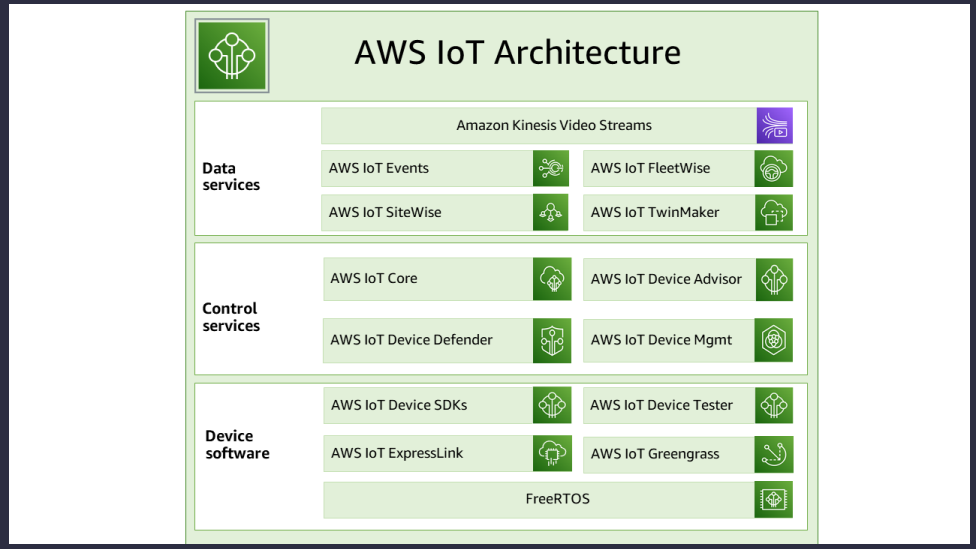
Fenerbahce University

How IoT Systems Work (End-to-End)

A practical mental model: device → network → edge/gateway → cloud → dashboard → actions



Edge–Fog–Cloud reference diagram

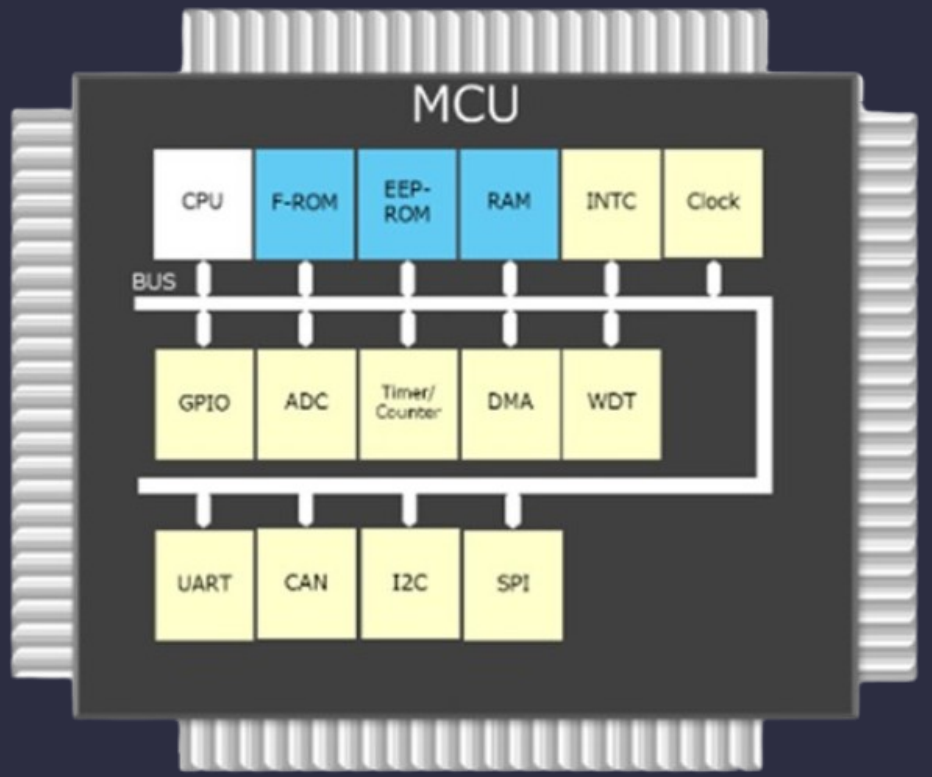


Example: AWS IoT “how it works” overview

MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - A low-power, single-chip processor optimized for real-time control.
  - Typically includes built-in RAM and Flash memory, no external storage required.
  - Handles simple tasks, does not perform complex computations.
  - Average Frequency: 1 MHz - 500 MHz
  - Average FLOPS: 10 MFLOPS - 100 MFLOPS

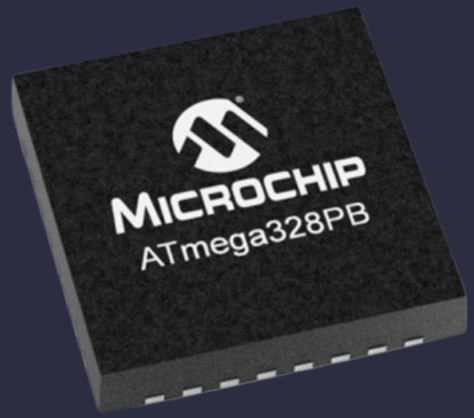


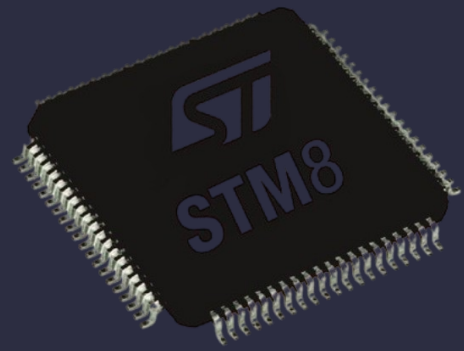
MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - MCU (Microcontroller Unit)

  - Vendors
    - Microchip Technology (PIC, AVR)
    - ST Microelectronic (STM8)
    - Texas Instruments (MSP430)
    - Renesas Electronics (RL78)

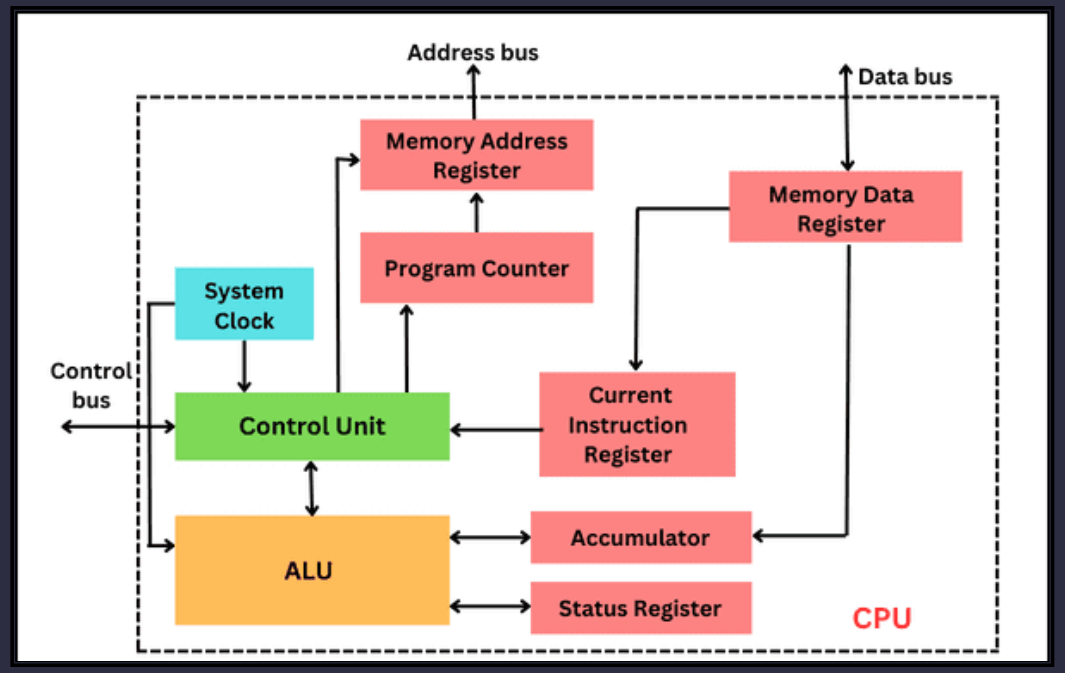


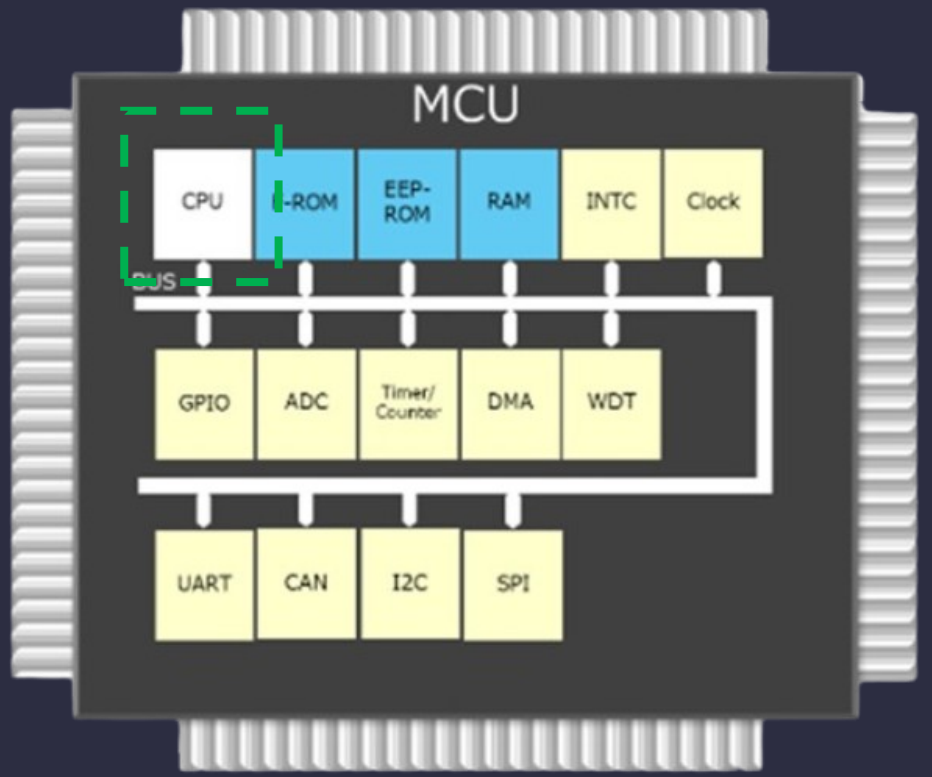


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - CPU Core

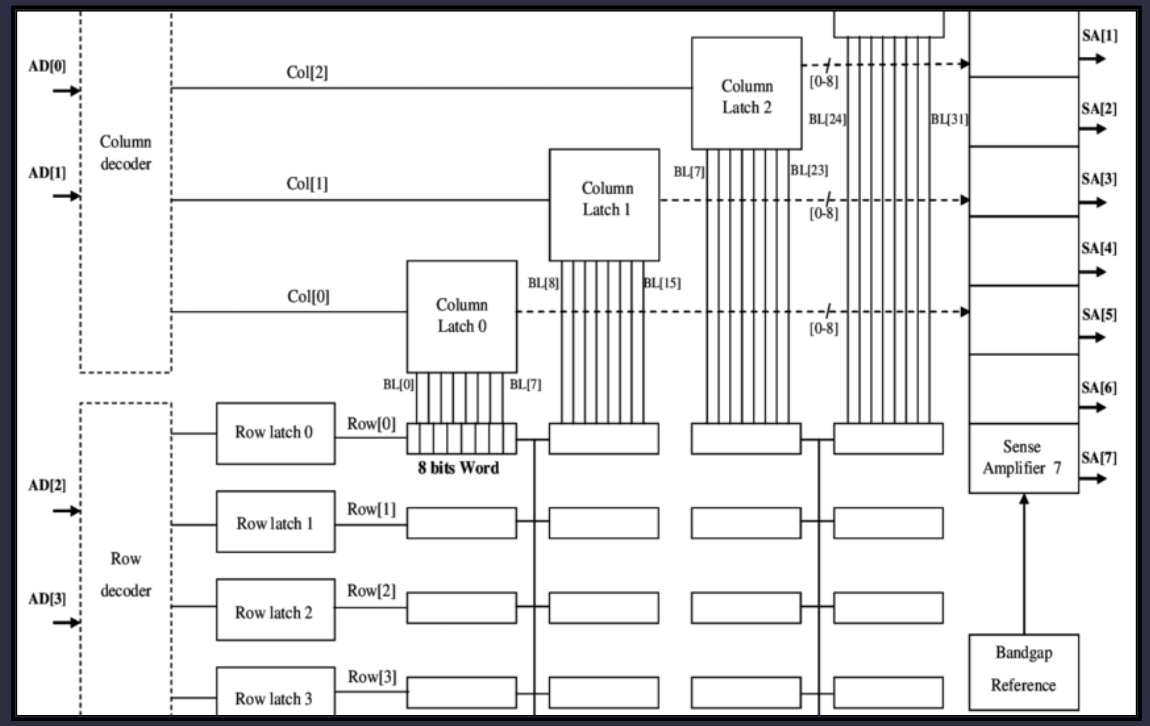


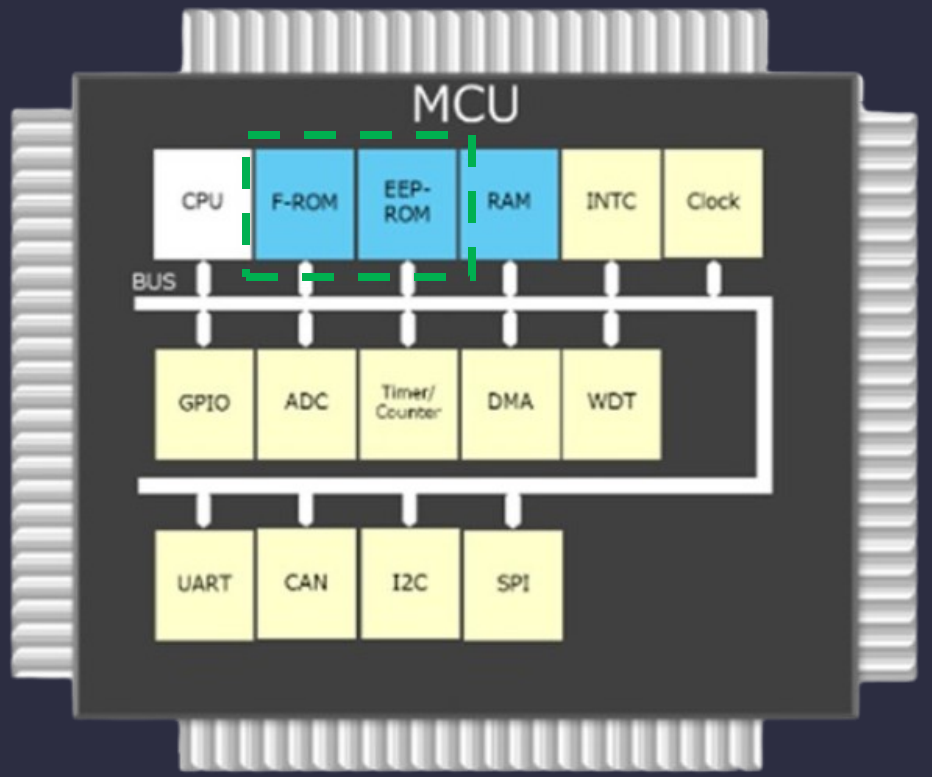


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - Memories (EEPROMs)

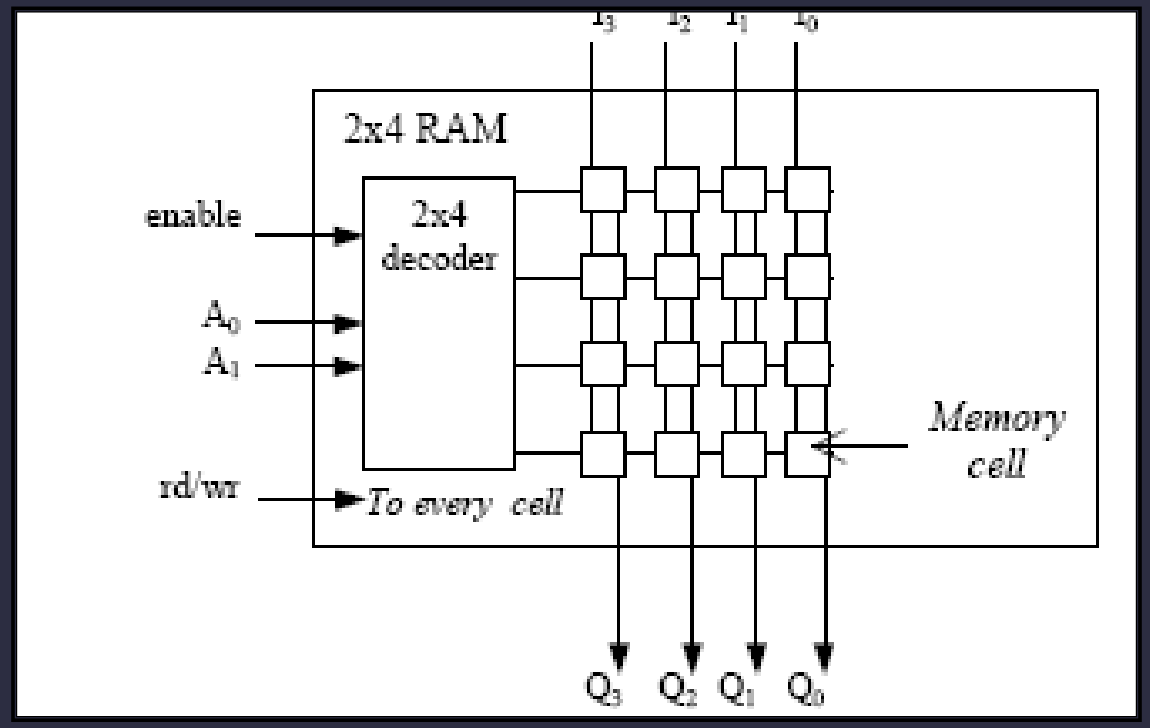


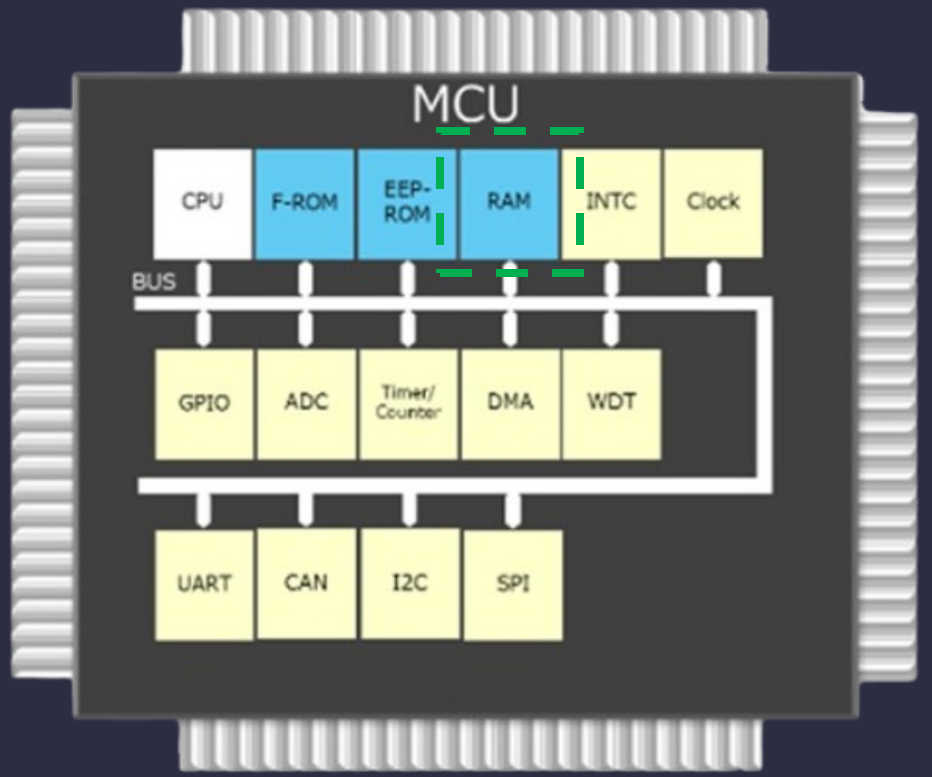


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - RAMs

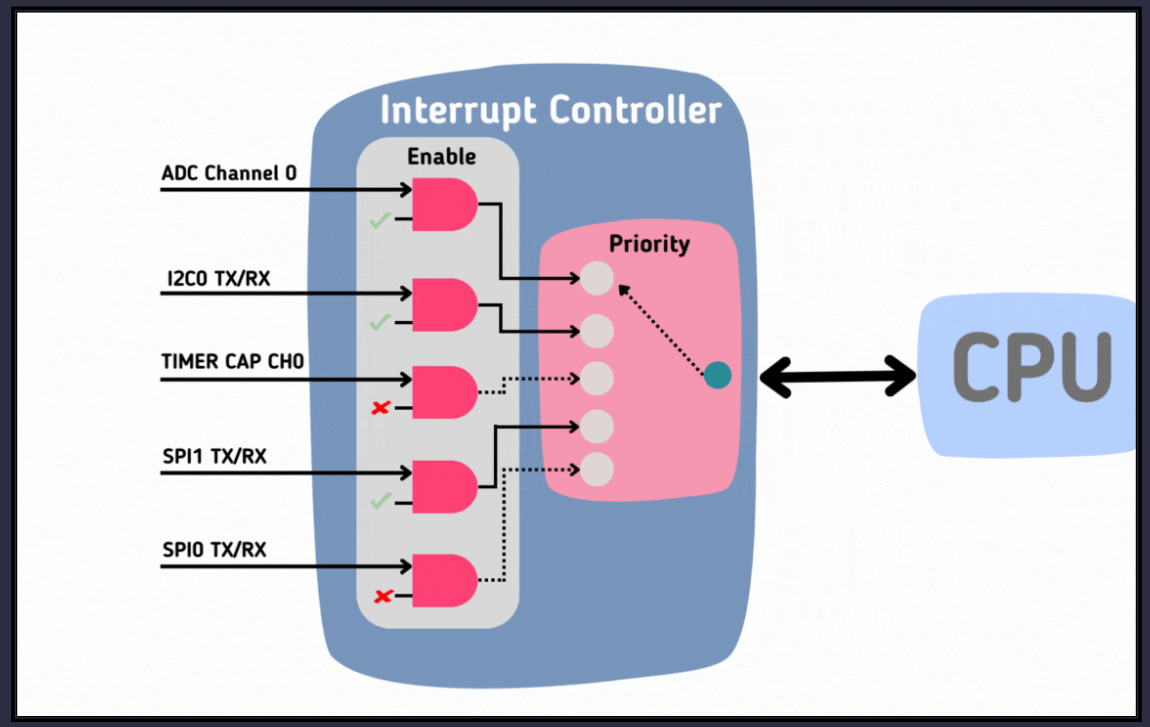


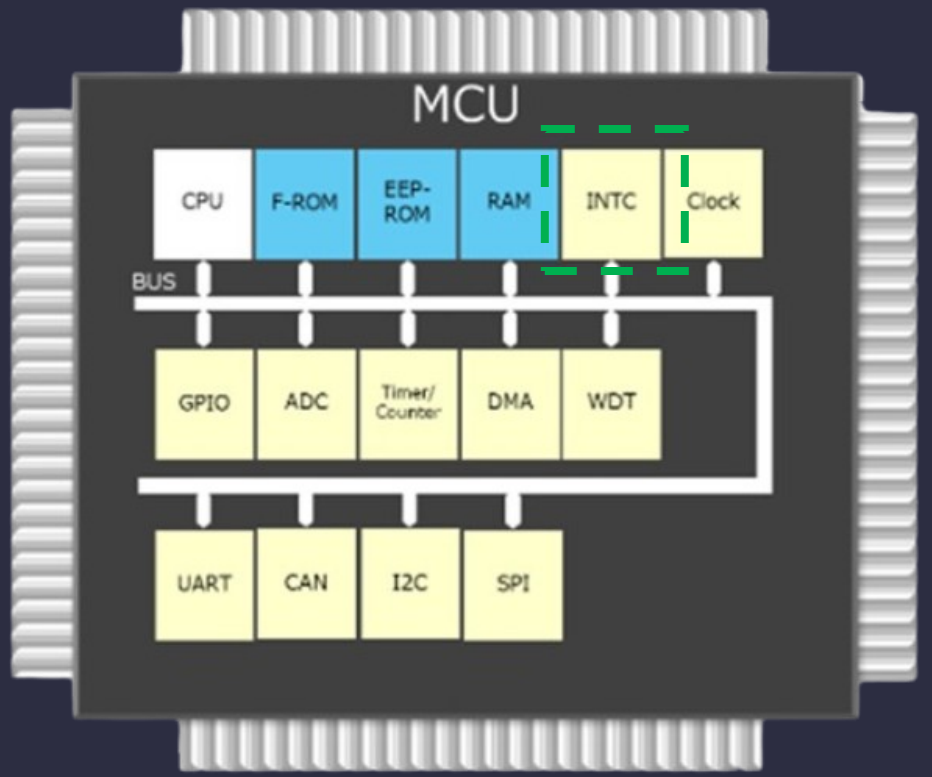


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

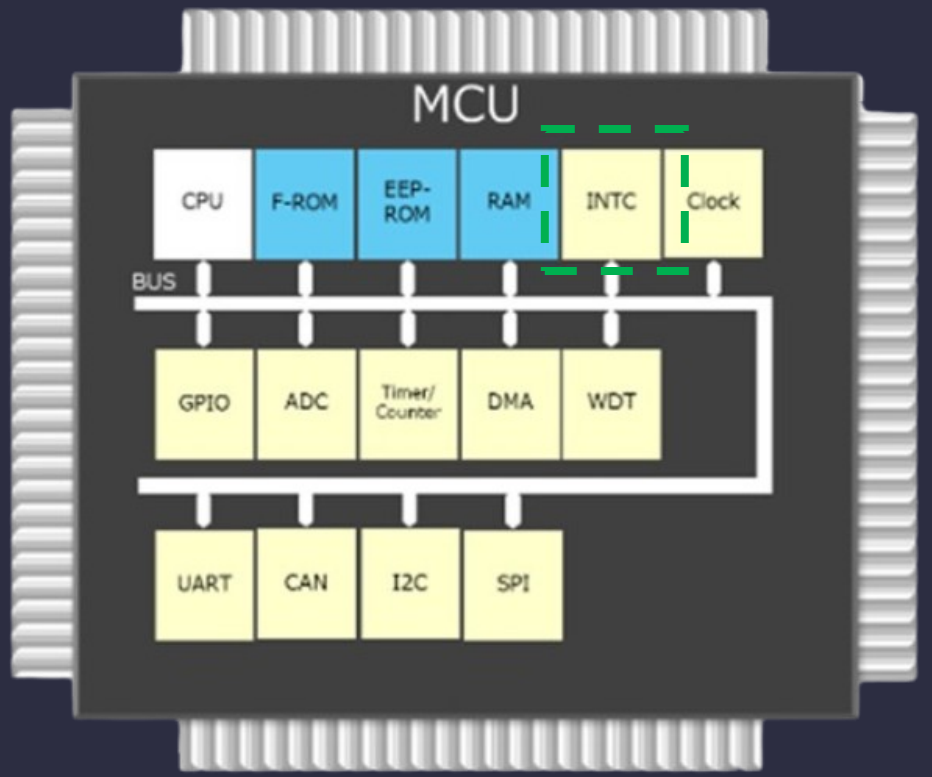
  - Interrupt Controllers (INTC)



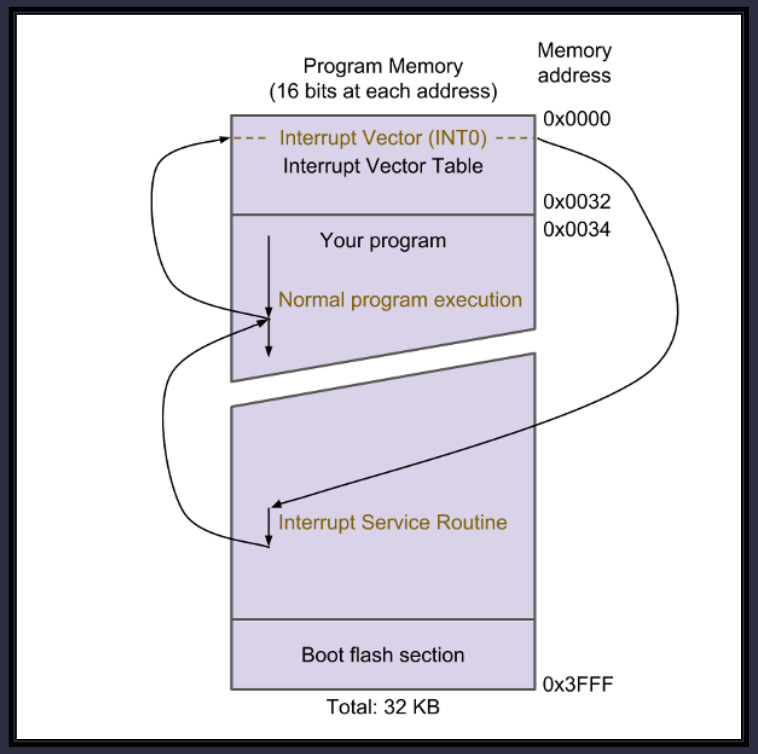


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

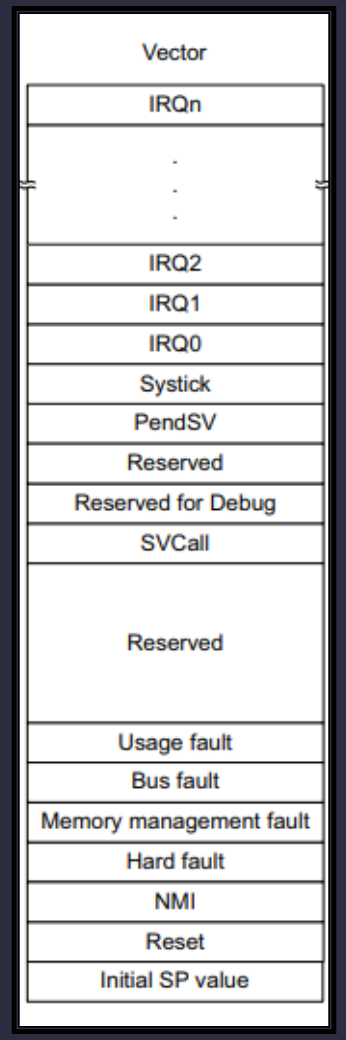


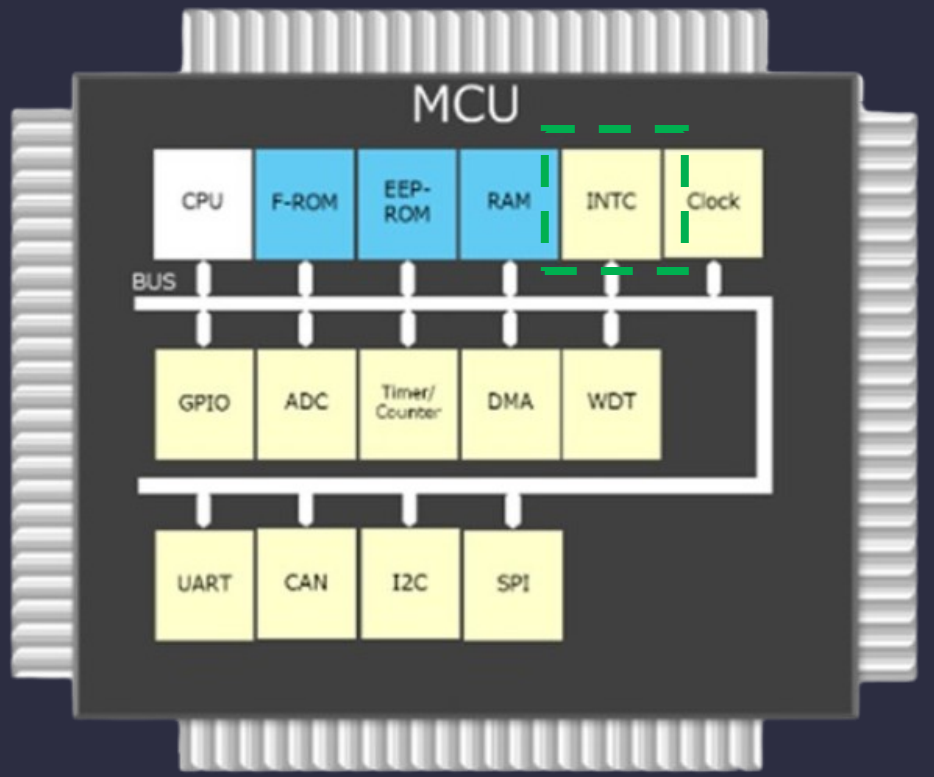
- Interrupt Controllers (INTC)



MCU & MPU Architectures, Interfaces

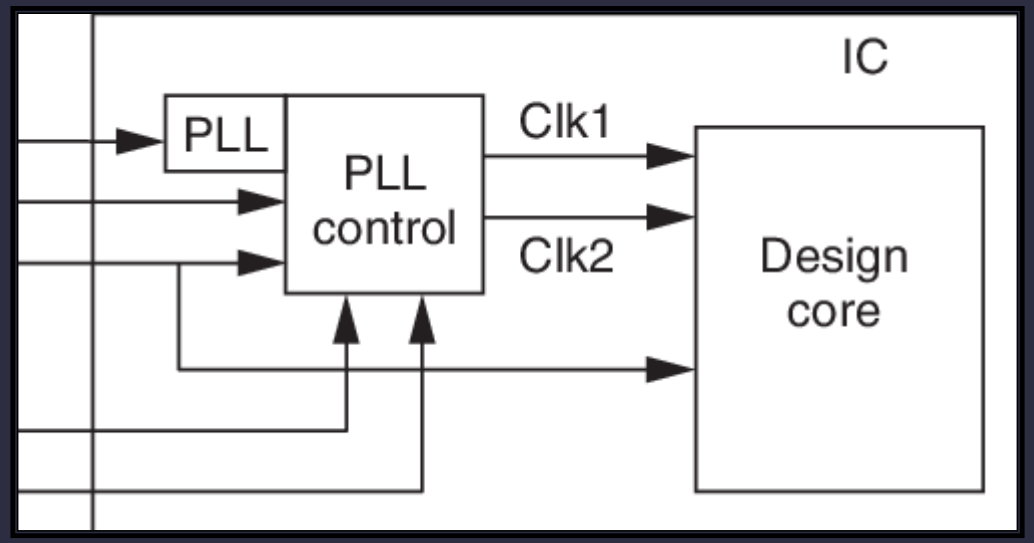
- Microcontroller Unit
  - Interrupt Controllers (INTC)
  - Interrput Vector

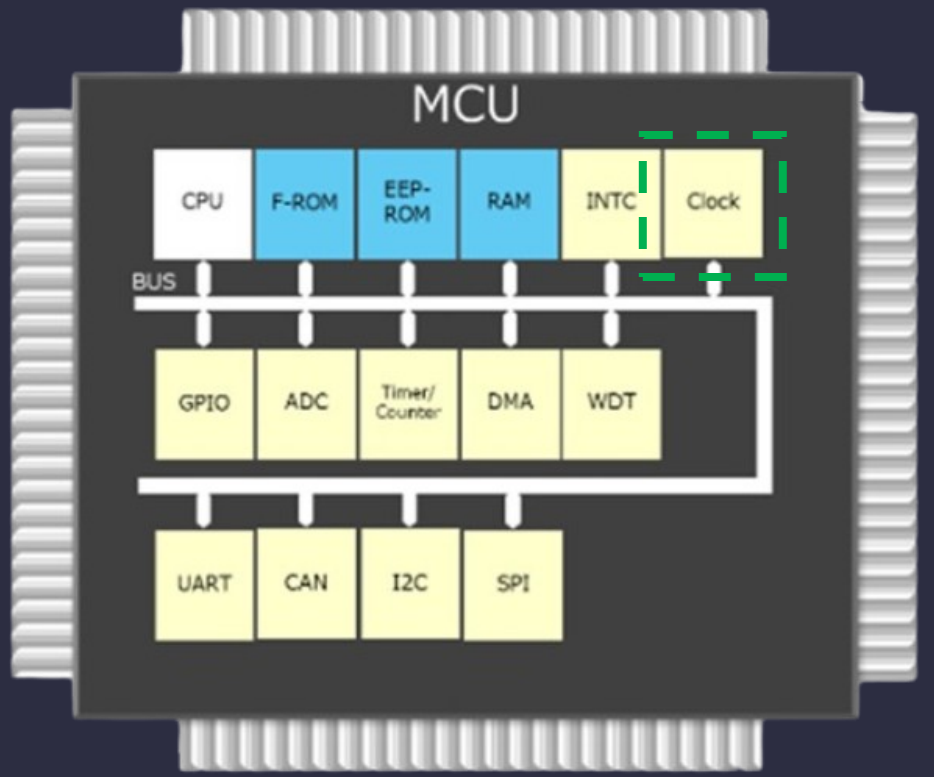




MCU & MPU Architectures, Interfaces

- Microcontroller Unit
  - Clock

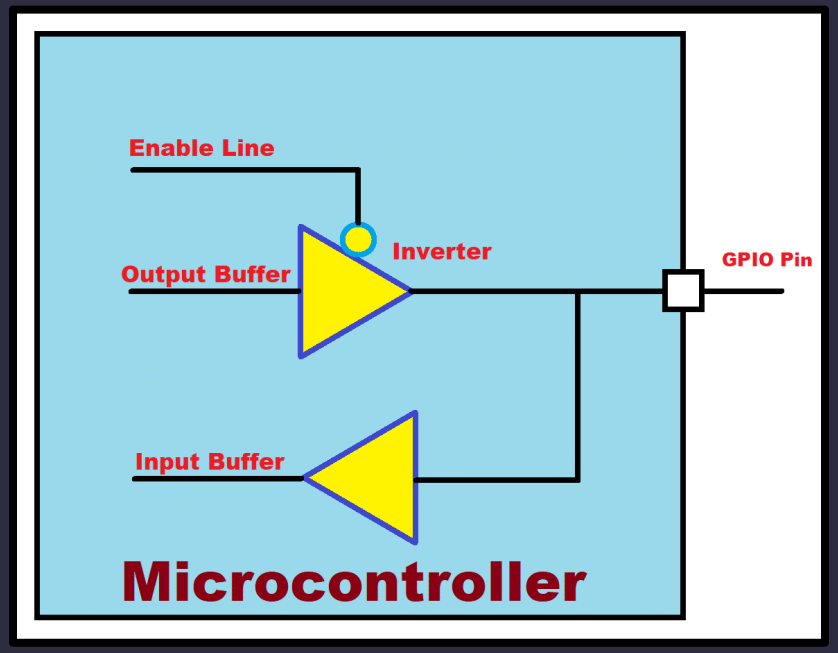


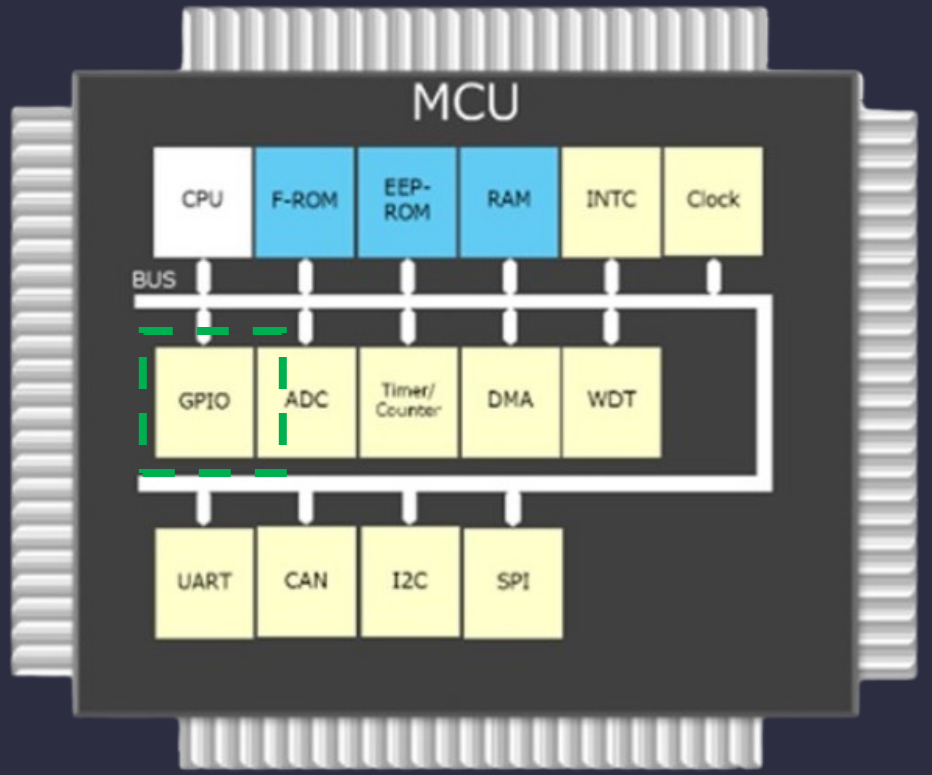


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - General Purpose Input/Output

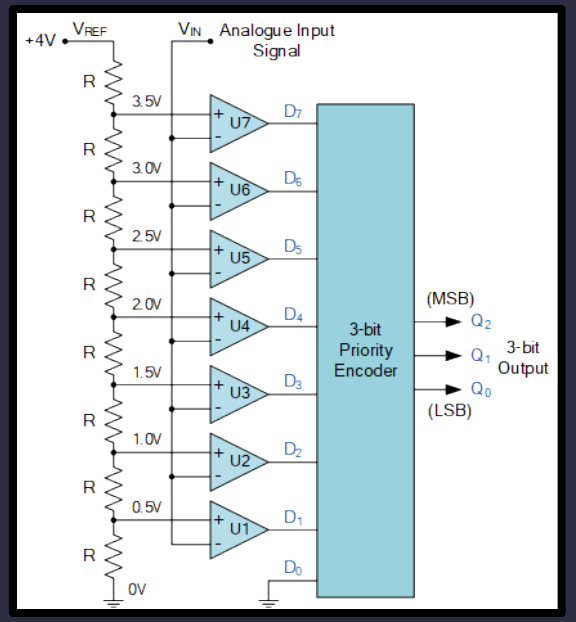




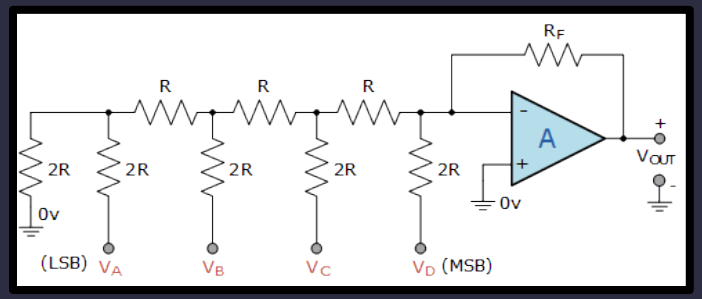
MCU & MPU Architectures, Interfaces

- Microcontroller Unit

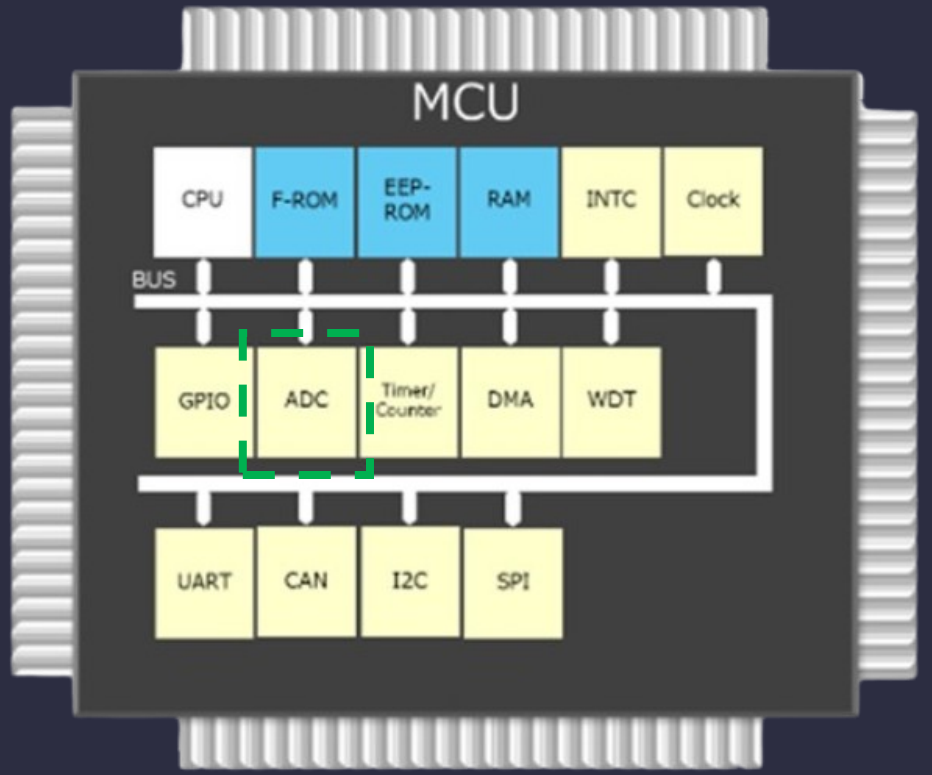
  - Analog Digital Converter or Digital Analog Conveter



ADC



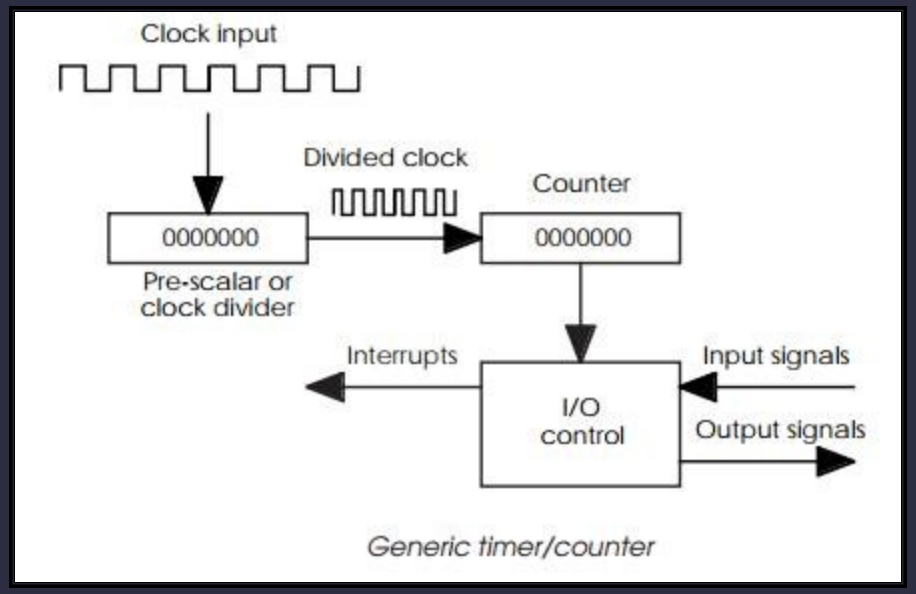
DAC

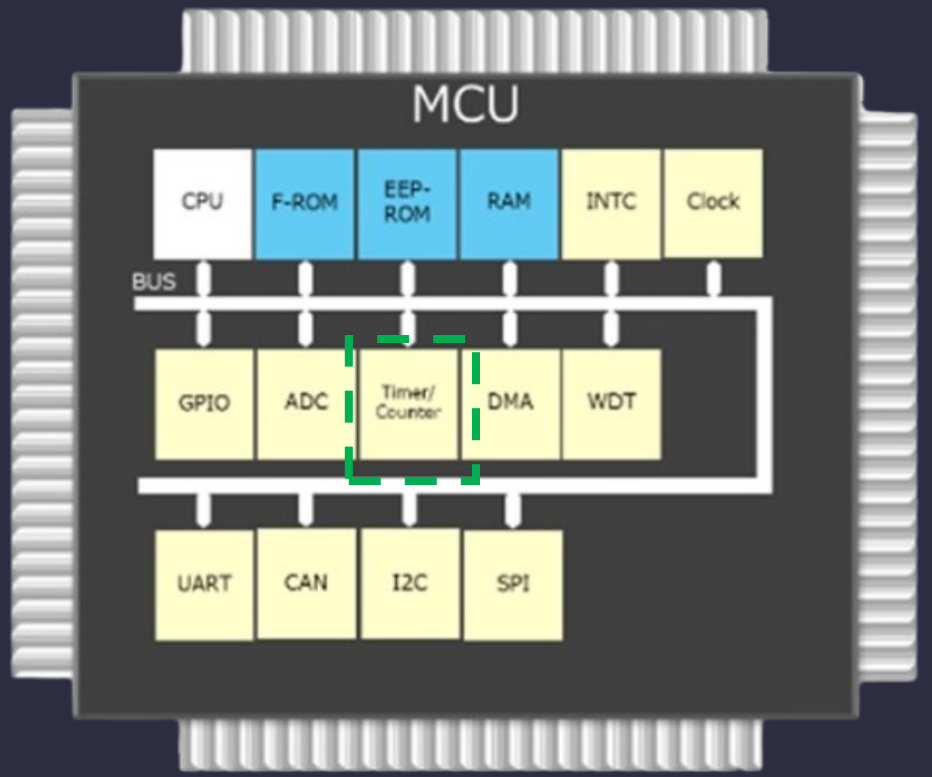


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - Timer/Counter

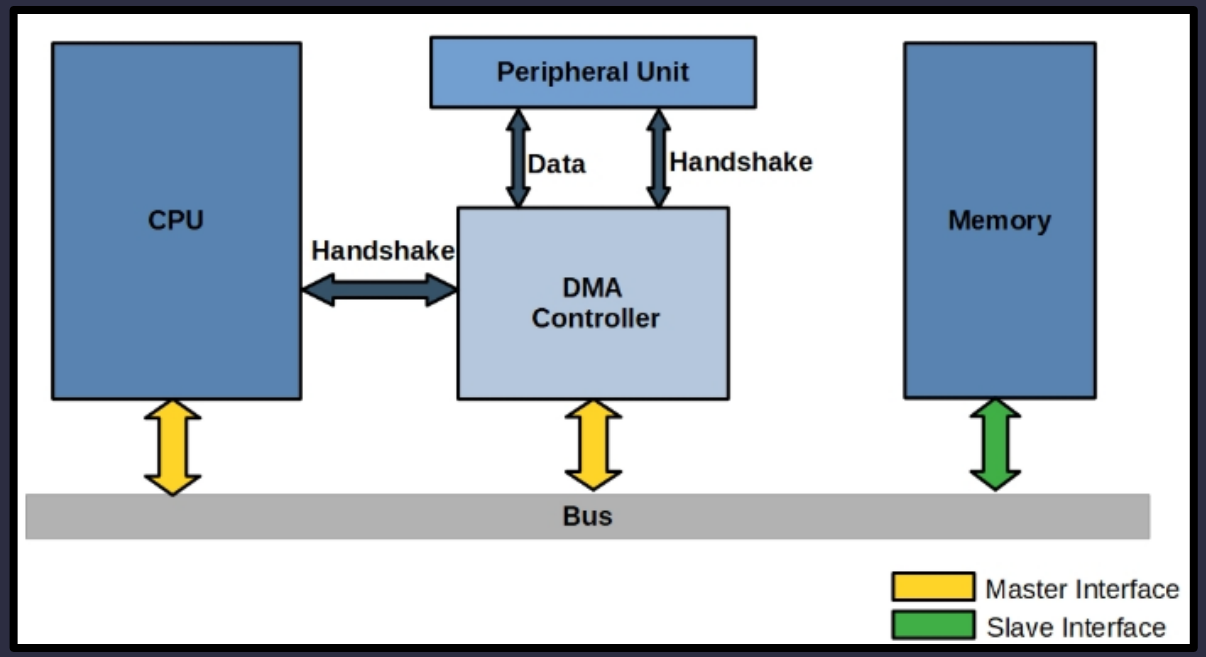


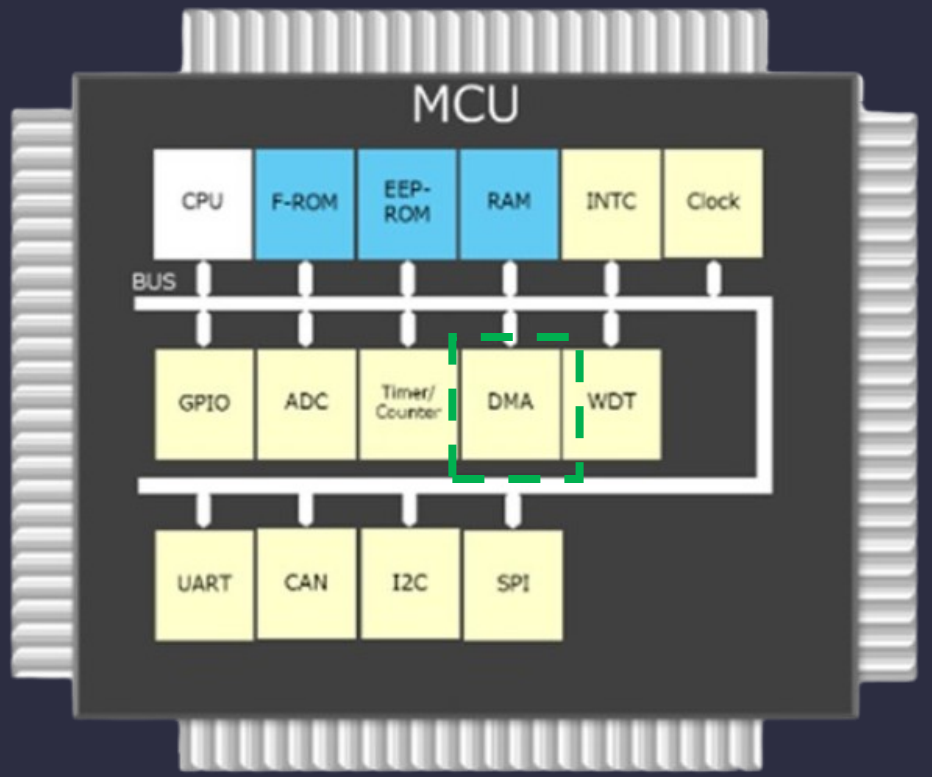


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - Direct Memory Access (DMA)

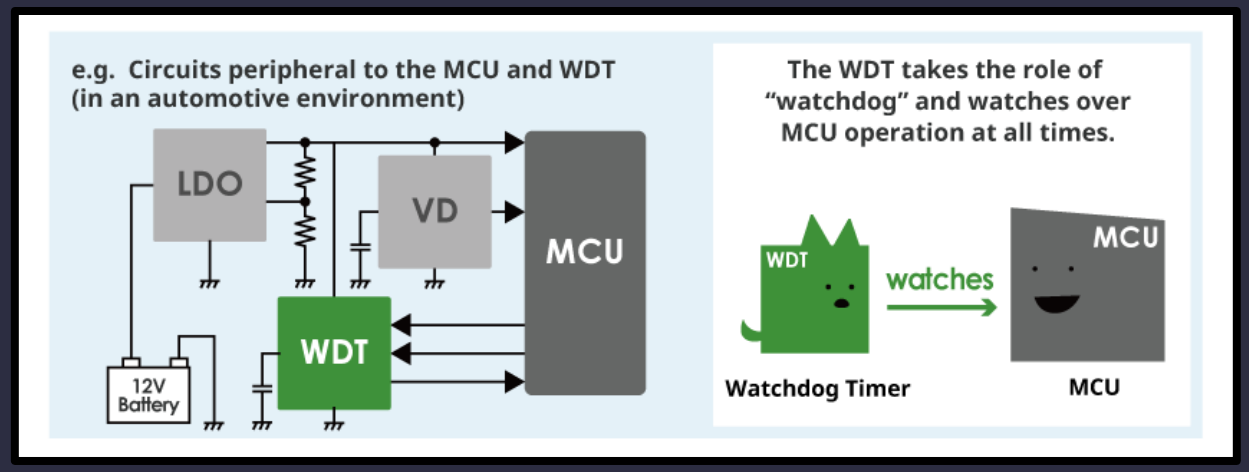


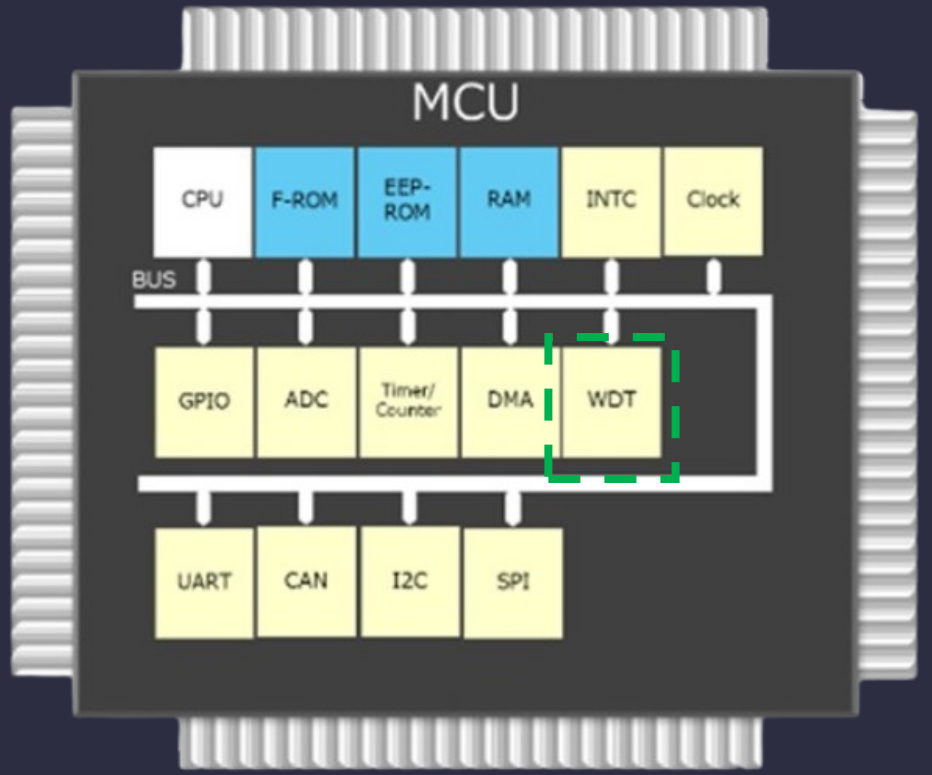


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - Watchdog Timer (WDT)

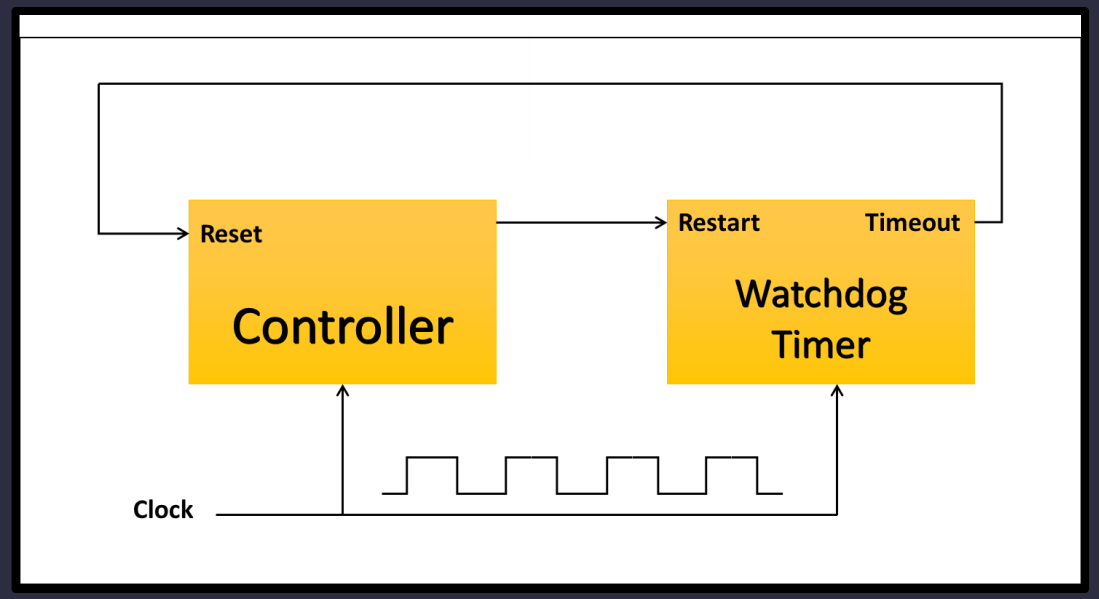


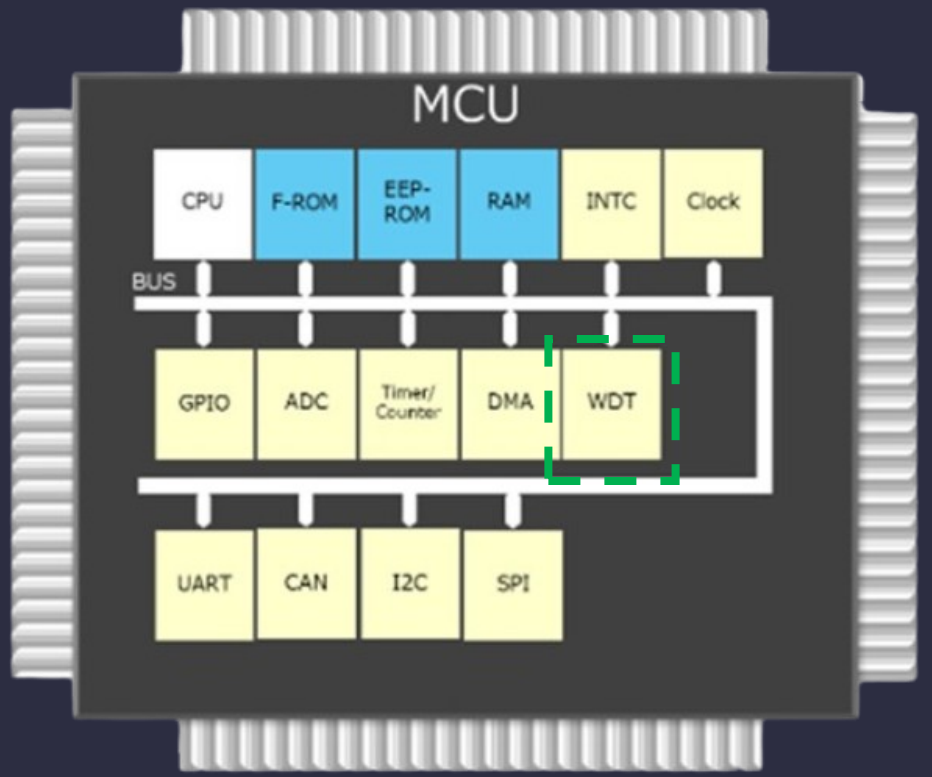


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

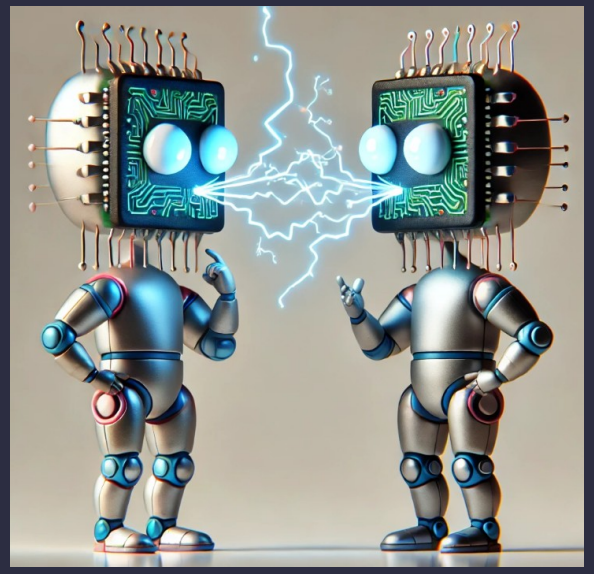
  - Watchdog Timer (WDT)

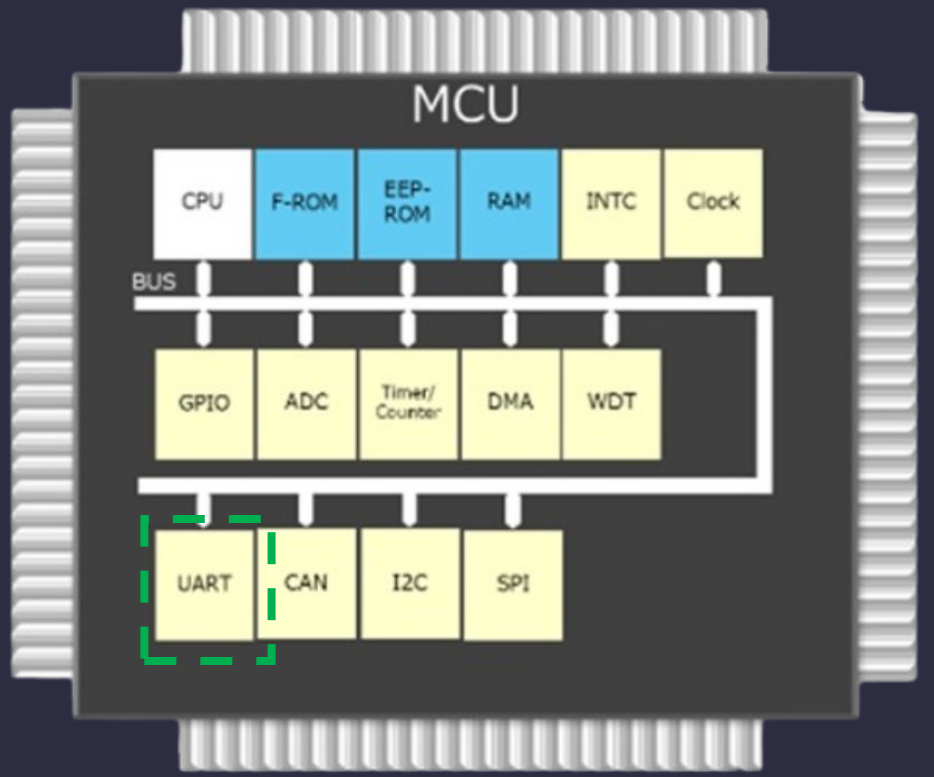




MCU & MPU Architectures, Interfaces

- Microcontroller Unit
  - Interfaces
  - Communication Standards





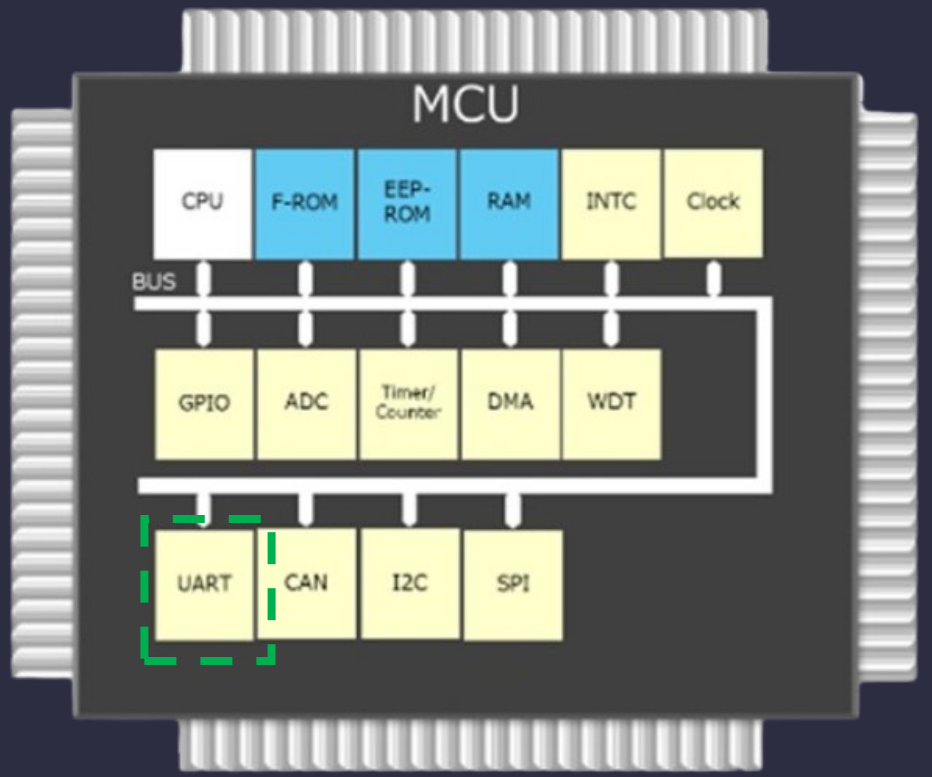
MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - Interfaces

  - Communication Standards
  - Commonly Using

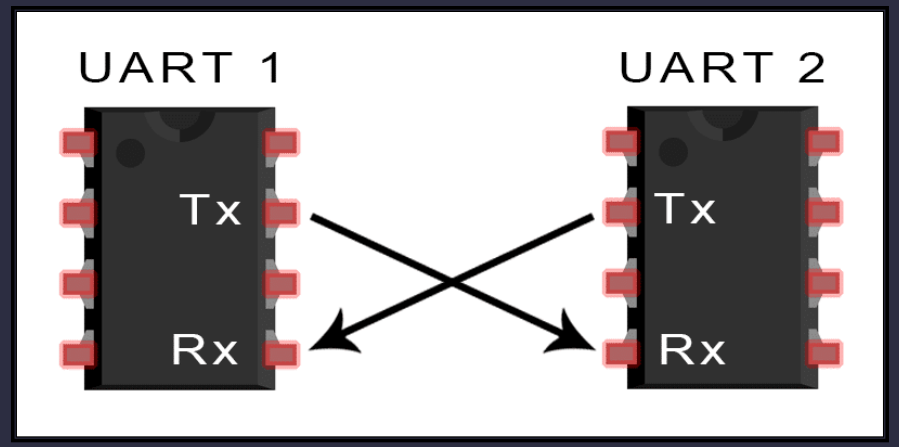
  - UART
  - CAN
  - I2C
  - SPI
  - Ethernet
  - PCI Express
  - …

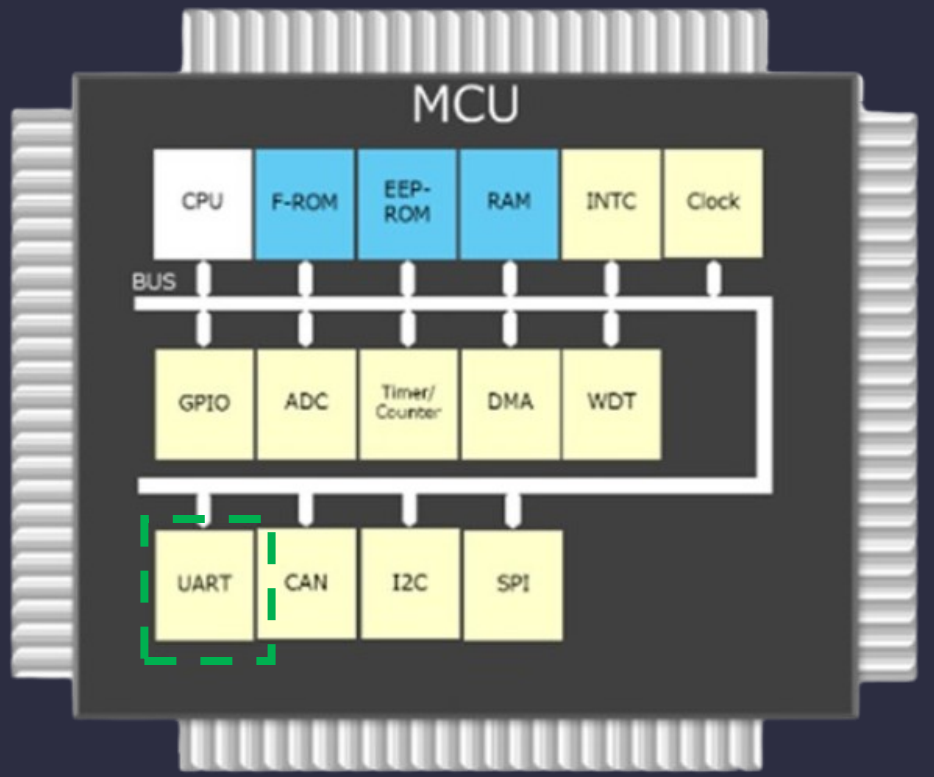


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

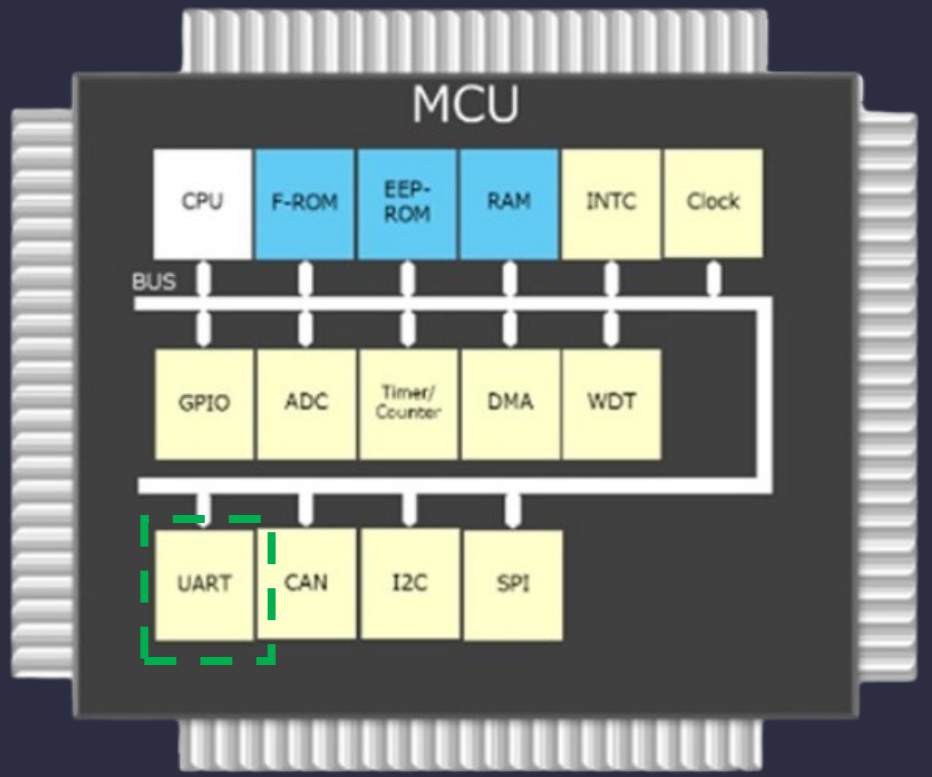
  - UART Interface
  - Communcates over two wires (RX and TX)





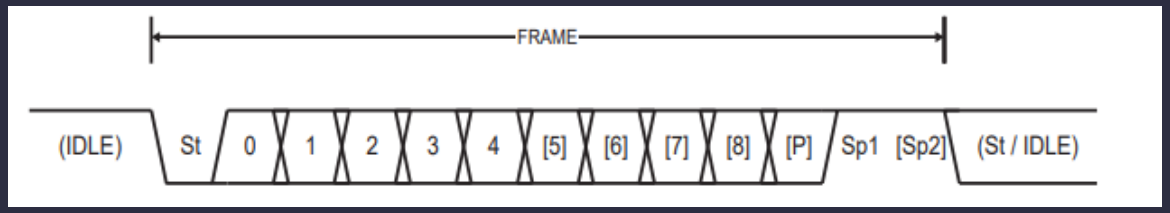
MCU & MPU Architectures, Interfaces

- Microcontroller Unit



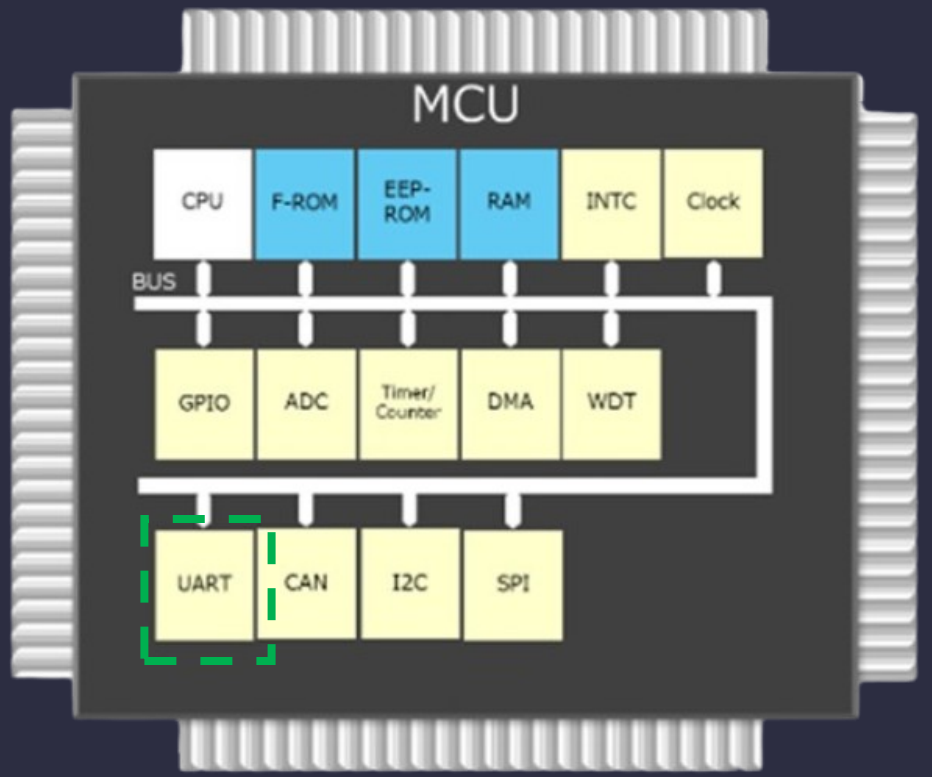
- UART Interface
- Packet Structure

- St Start bit, always low.
- (n) Data bits (0 to 8).
- P Parity bit. Can be odd or even.
- Sp Stop bit, always high.
- IDLE No transfers on the communication line (RxDn or TxDn). An IDLE line must be high.



MCU & MPU Architectures, Interfaces

- Microcontroller Unit



- UART Interface

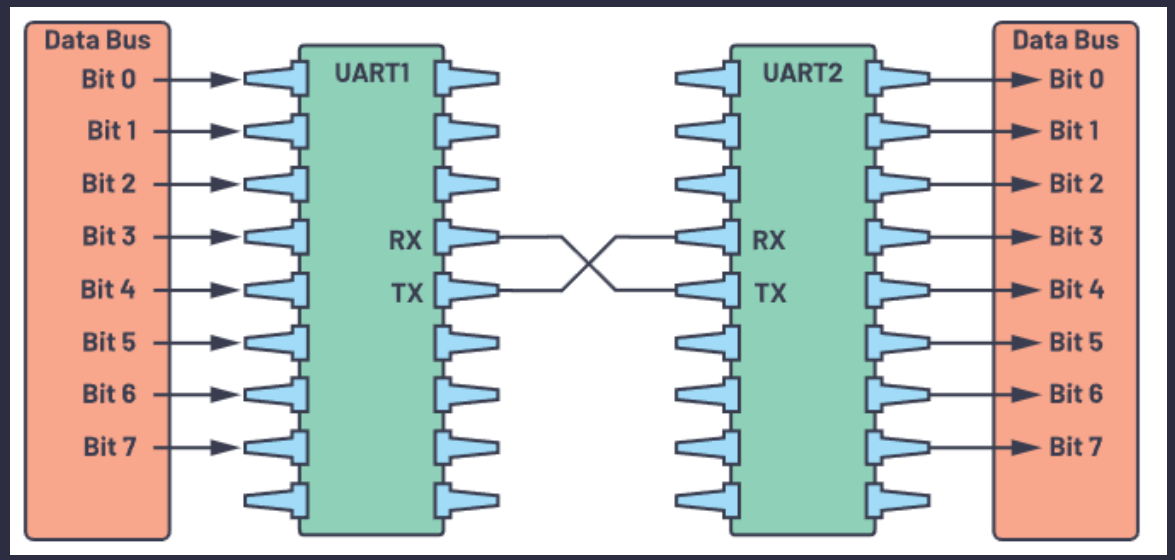
- Parity Bit Calculation
- The parity bit is calculated by doing an exclusive-or of all the data bits. If odd parity is used, the result of the exclusive or is inverted. The parity bit is located between the last data bit and first stop bit of a serial frame.
- The relation between the parity bit and data bits is as follows:

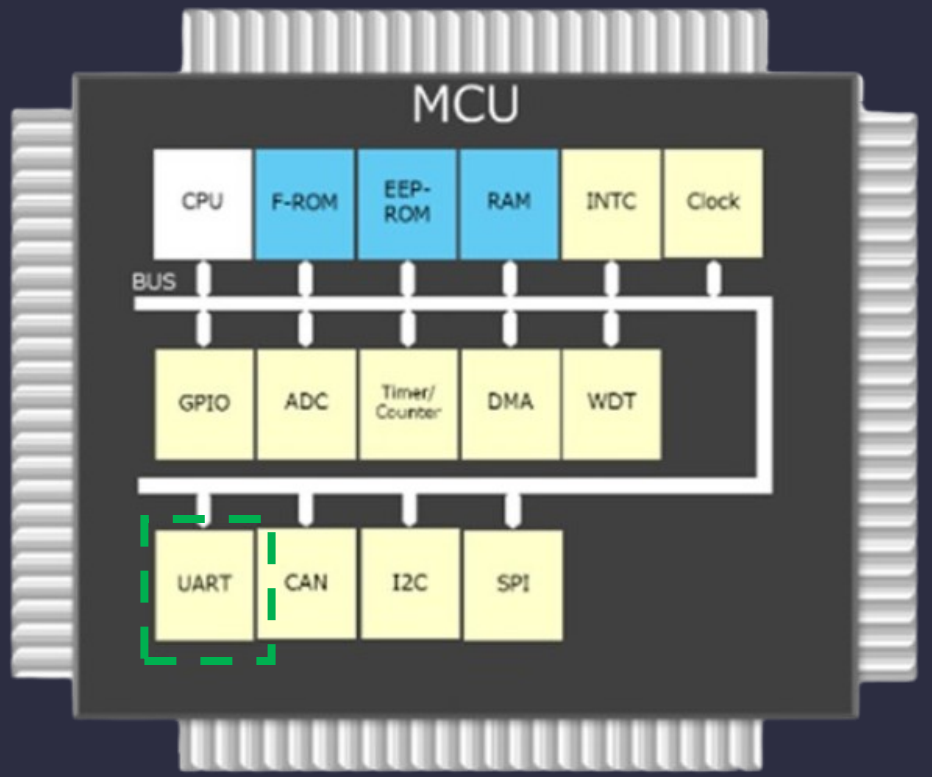
$$P_{even} = d_{n-1} \oplus \ldots \oplus d_3 \oplus d_2 \oplus d_1 \oplus d_0 \oplus 0$$
$$P_{odd} = d_{n-1} \oplus \ldots \oplus d_3 \oplus d_2 \oplus d_1 \oplus d_0 \oplus 1$$

P_{even}	Parity bit using even parity.
P^{odd}	Parity bit using odd parity.
d_n	Data bit n of the character.

MCU & MPU Architectures, Interfaces

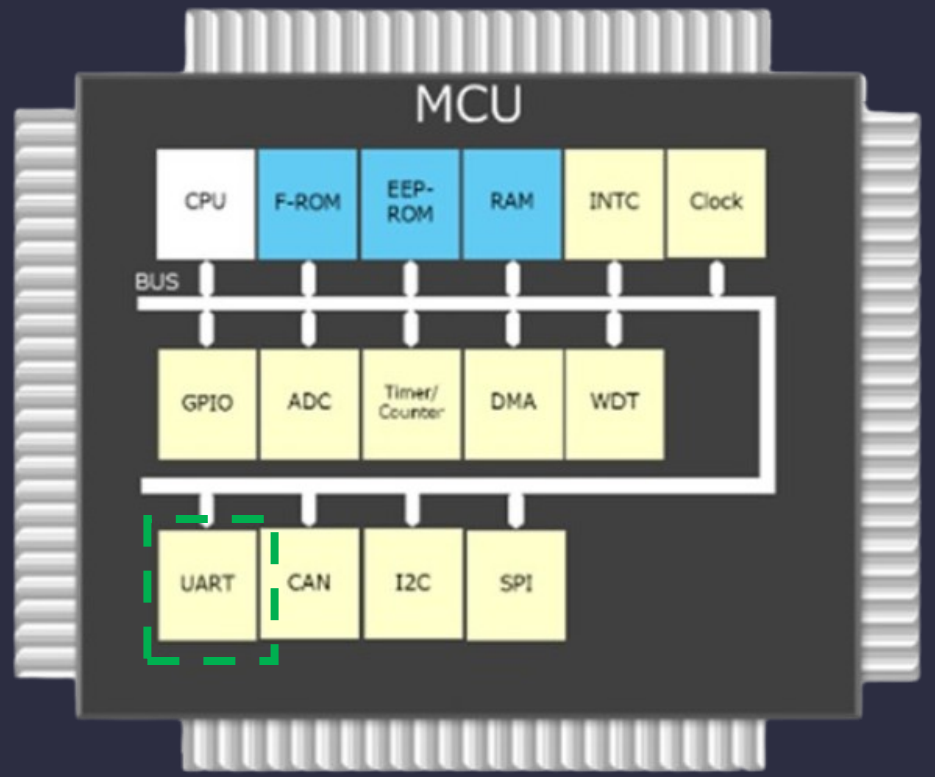
- Microcontroller Unit
  - UART Interface
  - Example





MCU & MPU Architectures, Interfaces

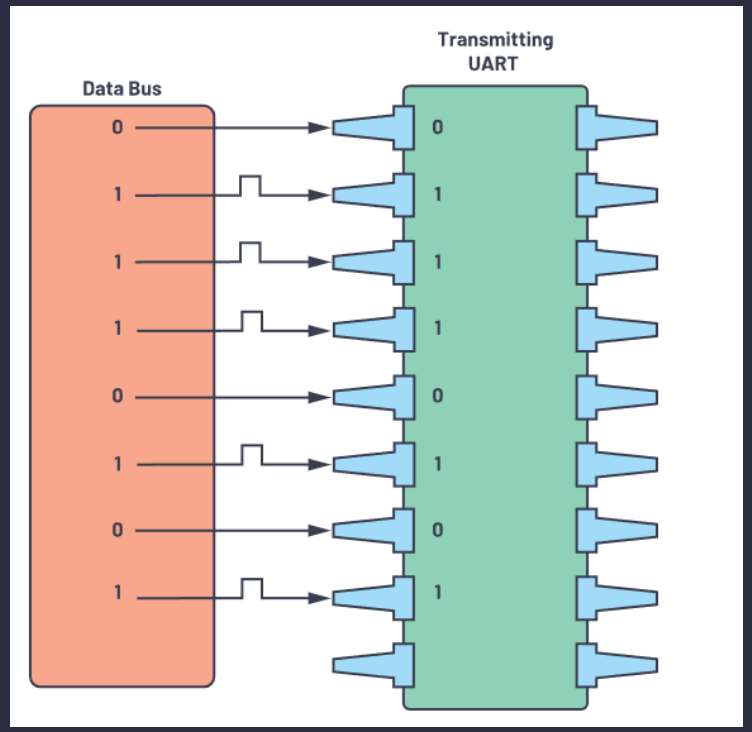
- Microcontroller Unit



- UART Interface

- Example
- Transmit

  0xAE
  10101110
  MSB LSB



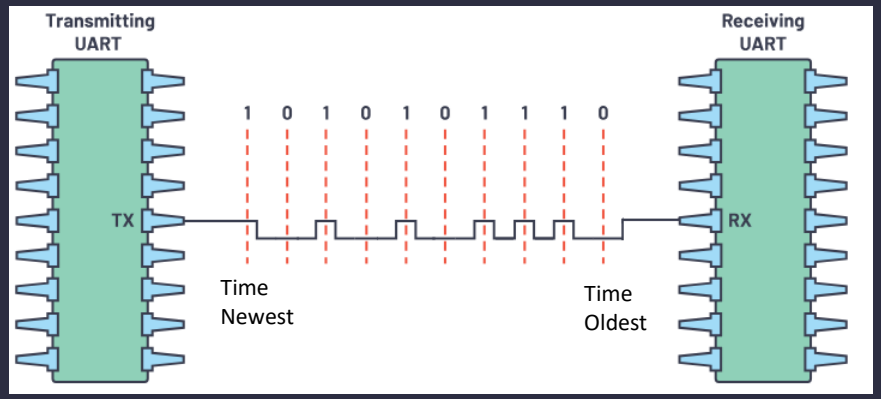
MCU & MPU Architectures, Interfaces

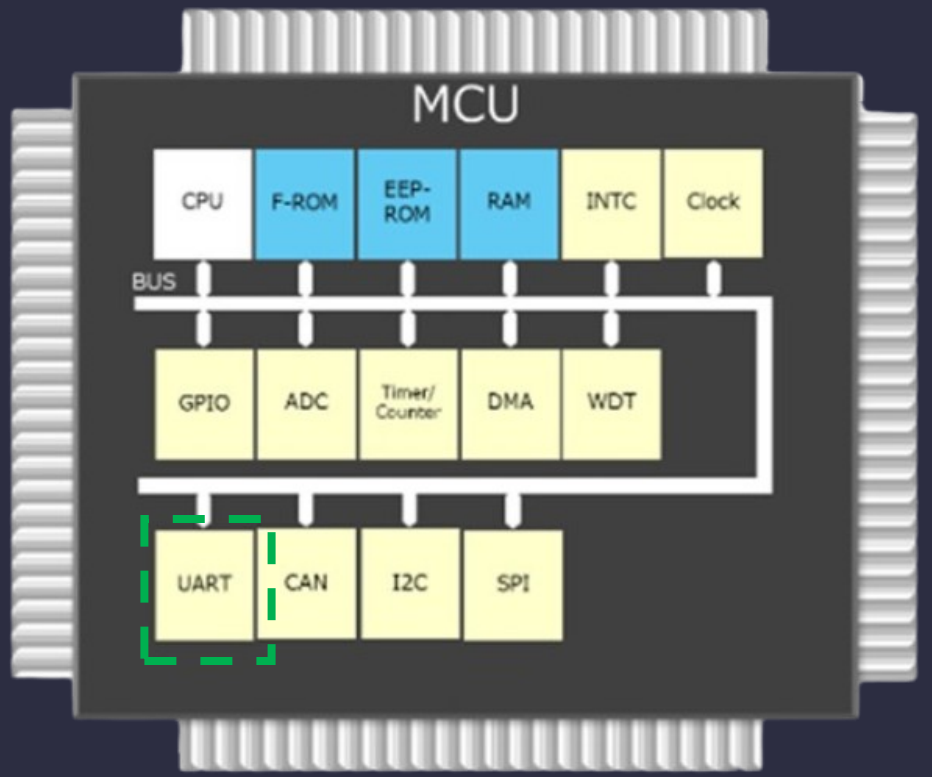
- Microcontroller Unit

  - UART Interface

  - Example
  - Transmit

    0xAE
    10101110
    MSB LSB





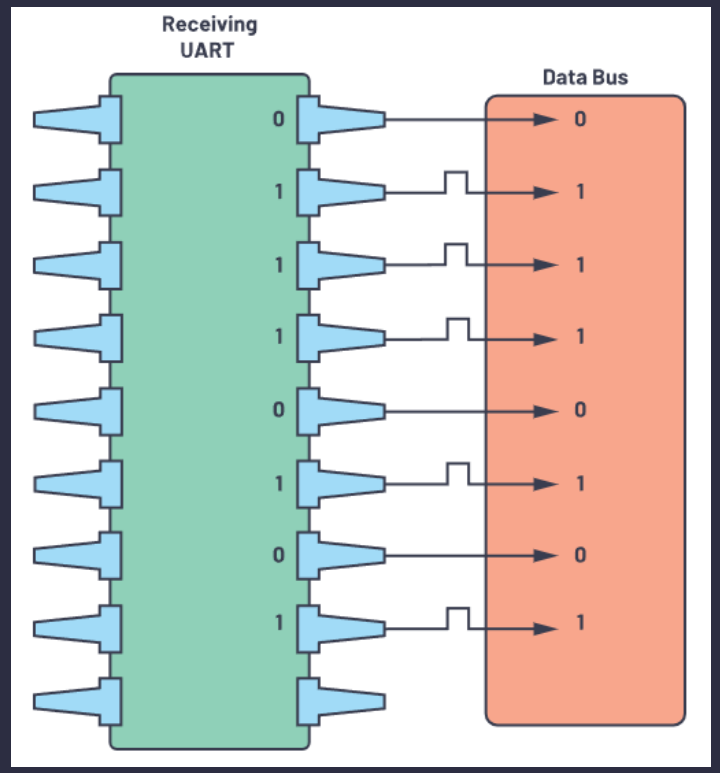
MCU & MPU Architectures, Interfaces

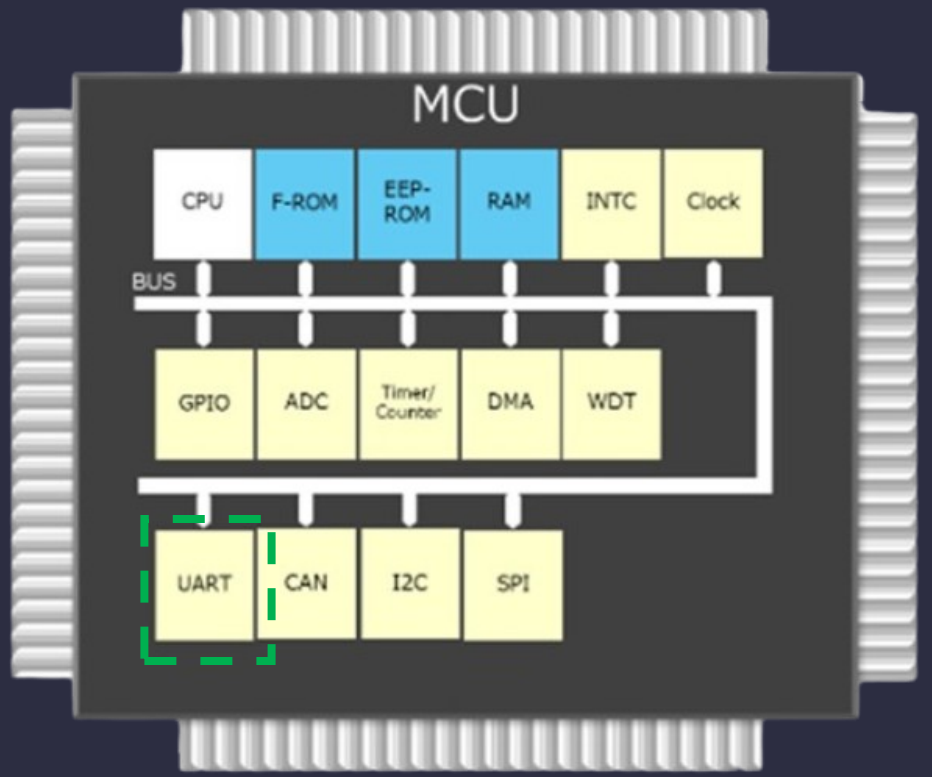
- Microcontroller Unit

  - UART Interface

  - Example
  - Transmit

    0xAE
    10101110
    MSB LSB





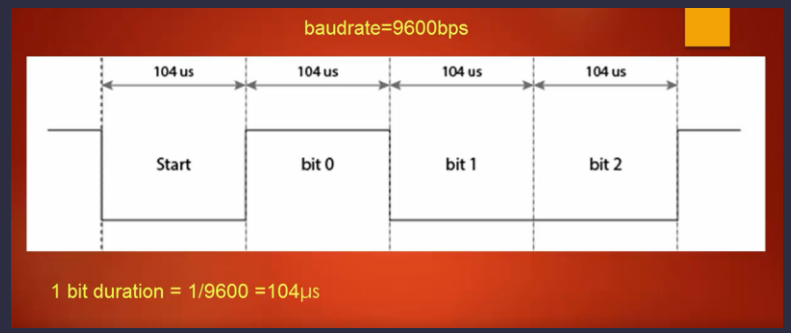
MCU & MPU Architectures, Interfaces

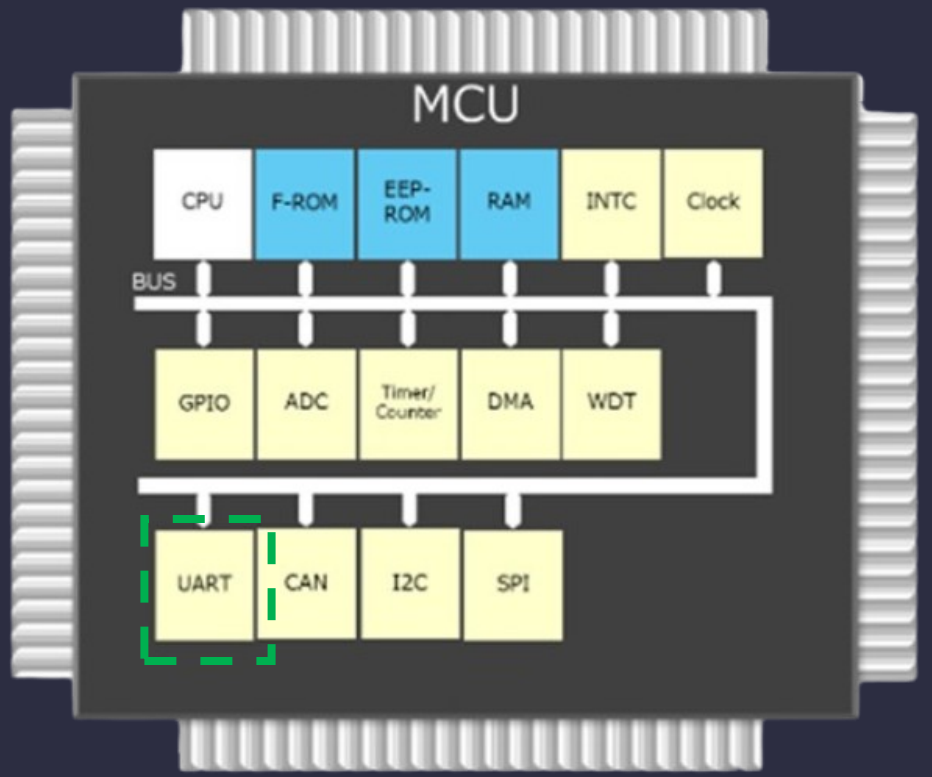
- Microcontroller Unit

  - UART Interface

  - Baud Rates (Speeds)

  - Commonly Using
    - 4800
    - 9600
    - 19200
    - 38400
    - 57600
    - 115200
    - 921600

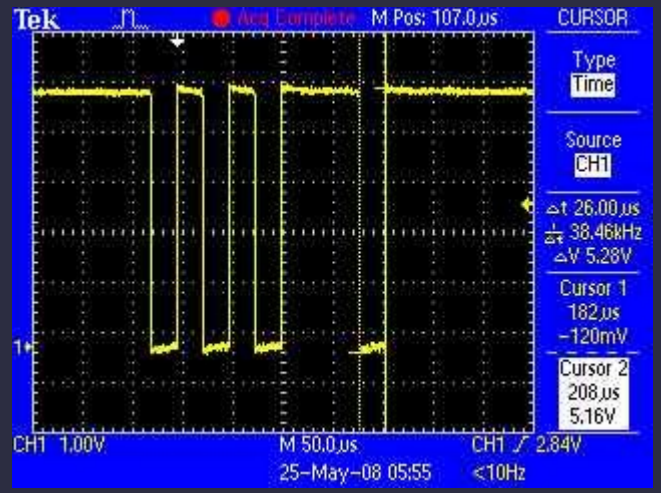


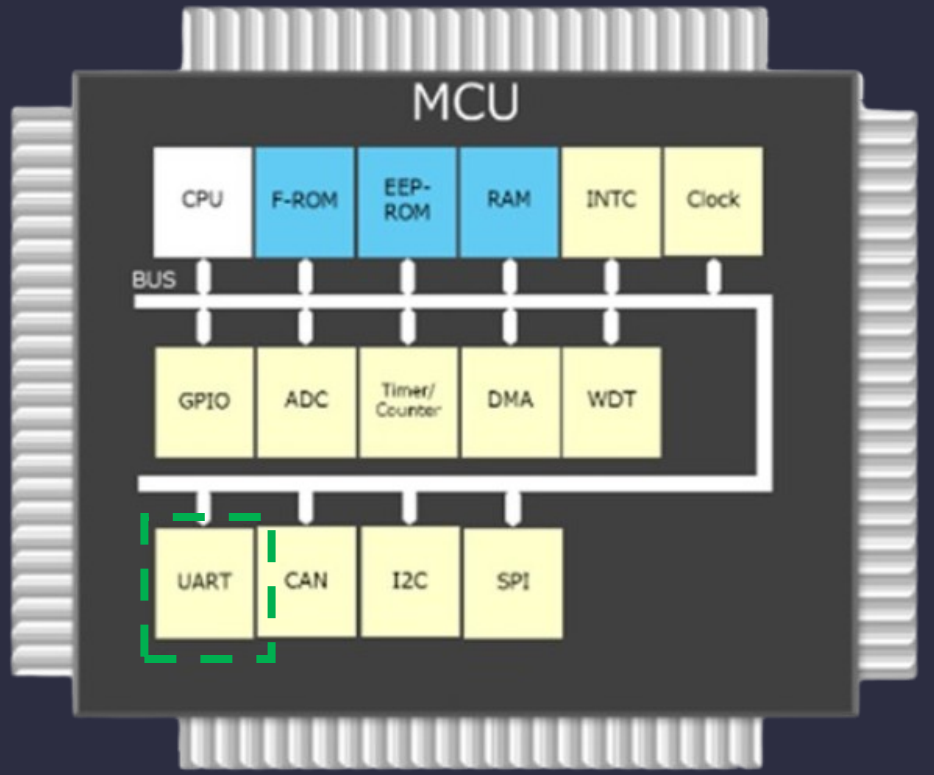


  - Effective data rate 8/10 (Due to Start & Stop Bits)
  - Ex for 9600 Baud Rate, Effectively 7680 (9600 * 0,8) Bits/S can be transmitted!

MCU & MPU Architectures, Interfaces

- Microcontroller Unit
  - UART Interface
  - Baud Rates (Speeds)
  - Commonly Using
    - 4800
    - 9600
    - 19200
    - 38400
    - 57600
    - 115200
    - 921600





- Diagram of 4800 Baud rate of UART Transmission
- Pulse time 208 micro seconds.

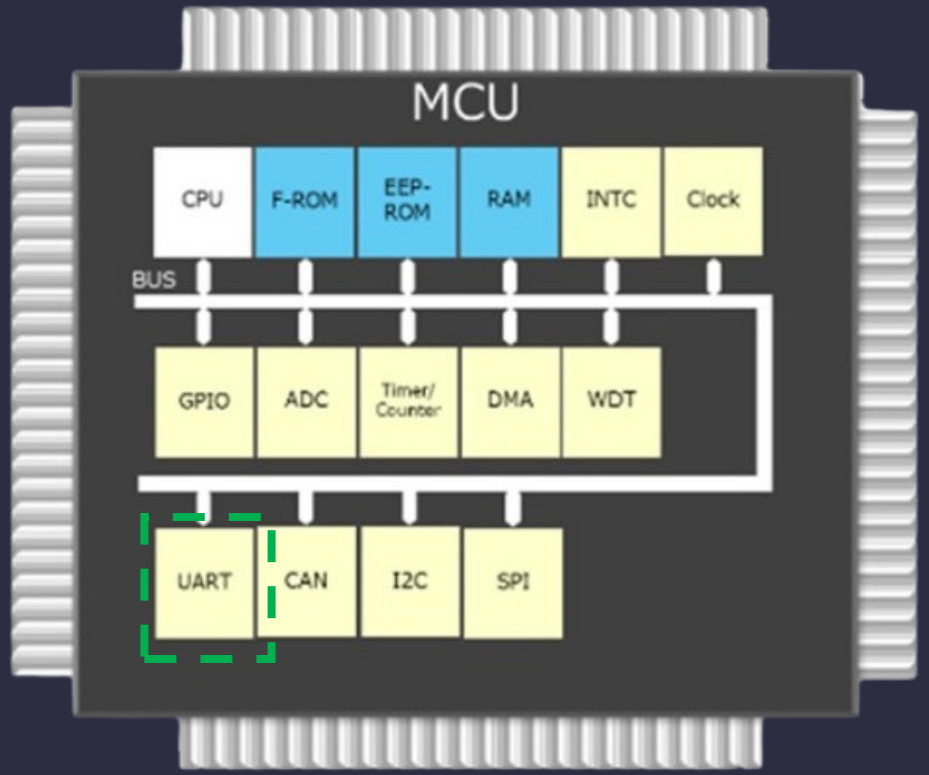
MCU & MPU Architectures, Interfaces

- Microcontroller Unit

- UART Interface
- Baud Rates (Speeds)
- Commonly Using
  - 4800
  - 9600
  - 19200
  - 38400
  - 57600
  - 115200
  - 921600

Time	Baud Rate
3333µs (3.3ms)	300
833µs	1200
416µs	2400
208µs	4800
104µs	9600
69µs	14400
52µs	19200
34µs	28800
26µs	38400
17.3µs	57600
8µs	115200
4.34µs	230400

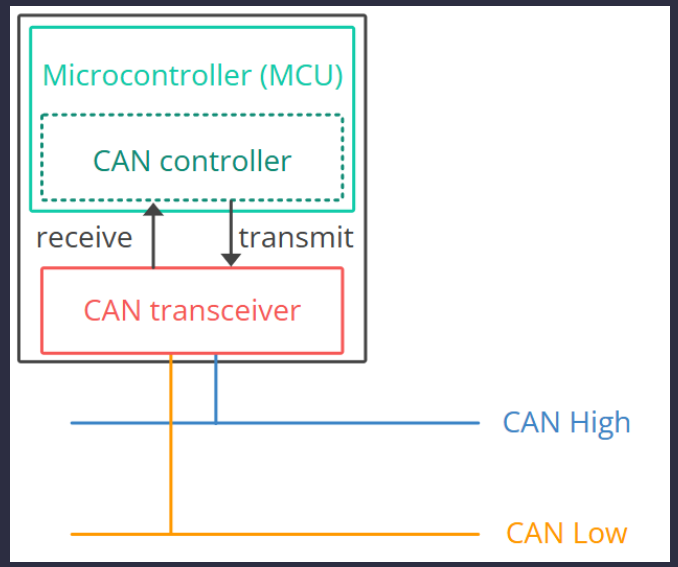
Table. Pulse Times

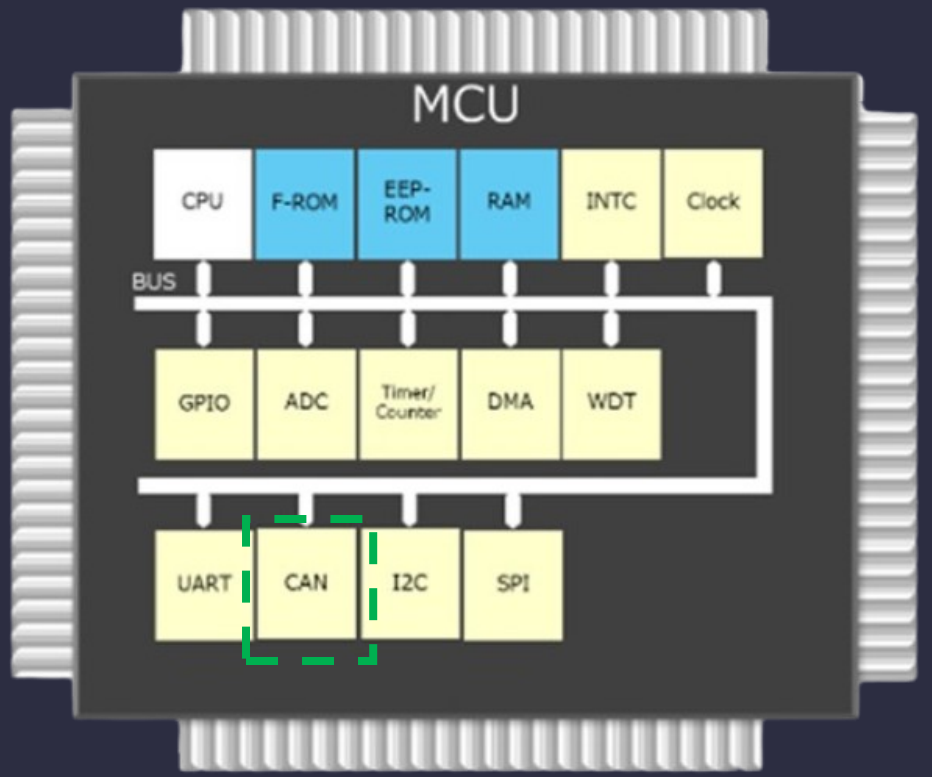


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - CAN (Control Area Network) Interface
  - Invented by Bosh, 1986
  - Last update on 2012
  - Differential Signalling
  - Mostly using in
    - Automotive
    - Medical
    - Robotics

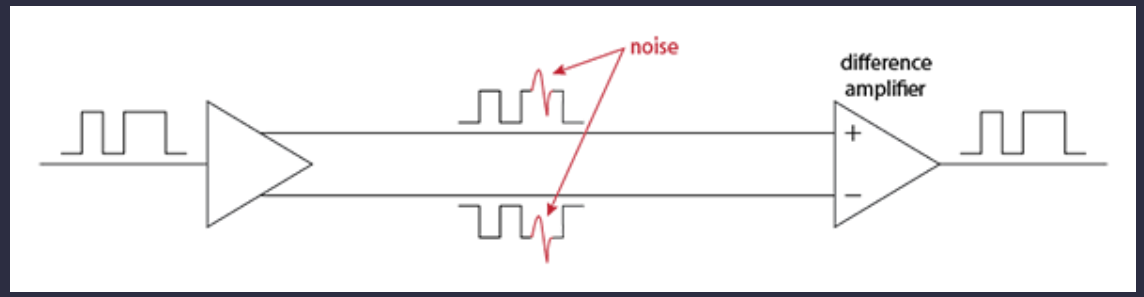


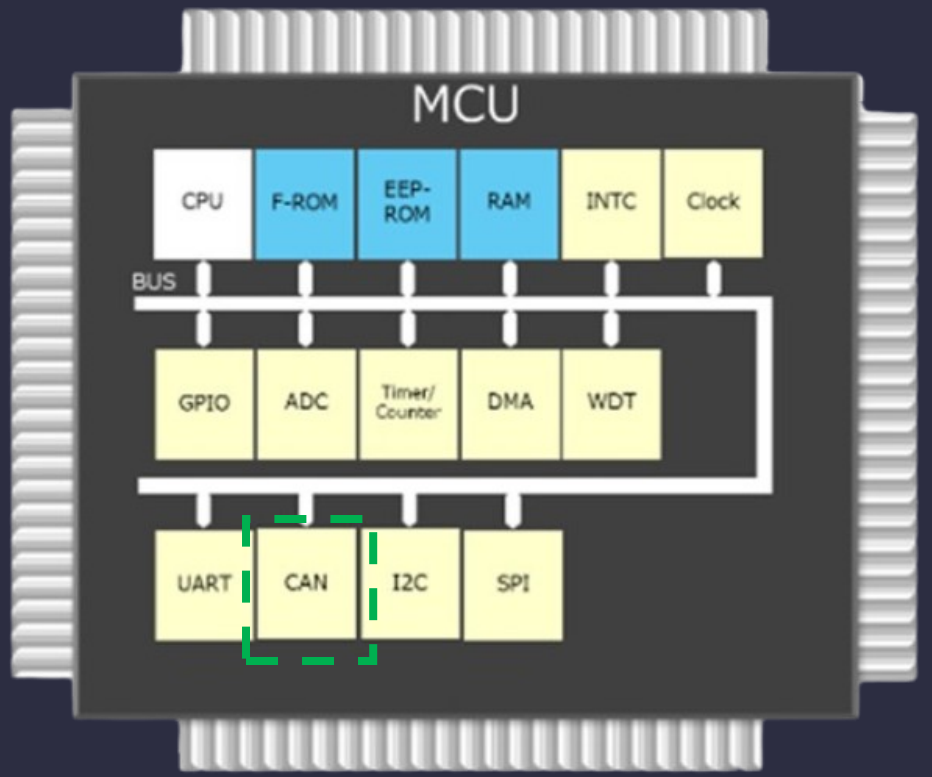


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - CAN (Control Area Network) Interface
  - Differential Signalling

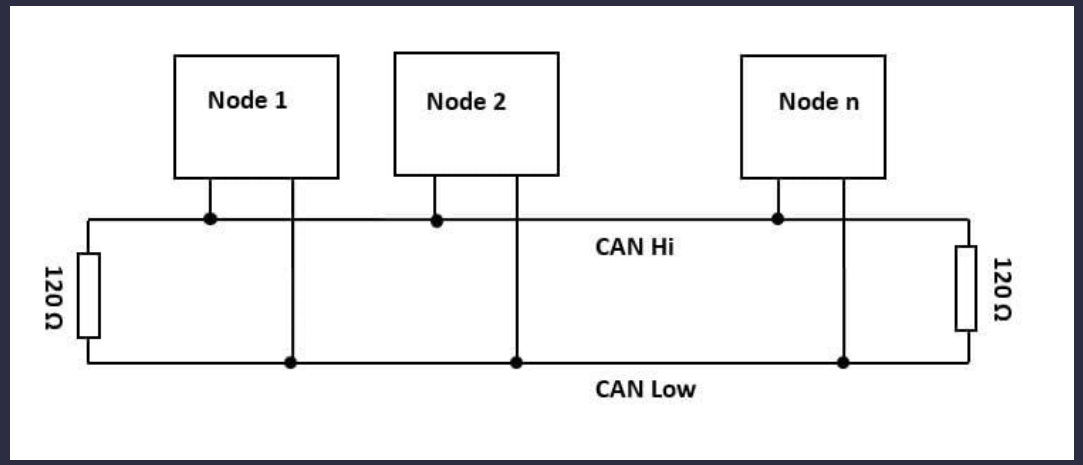


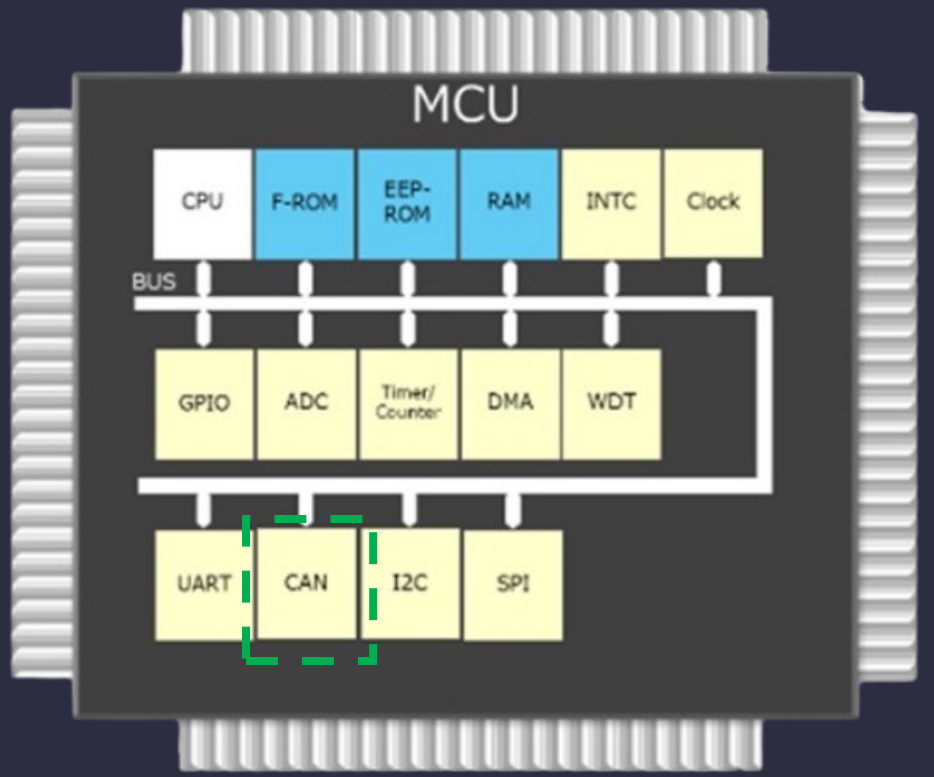


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - CAN (Control Area Network) Interface
  - Multiple Nodes

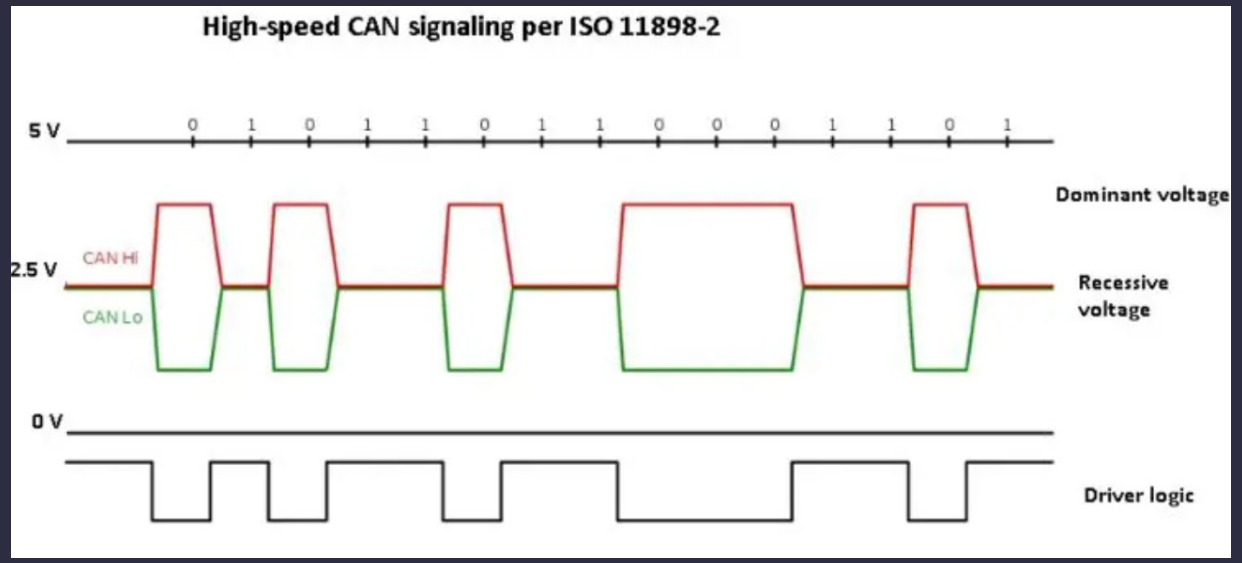


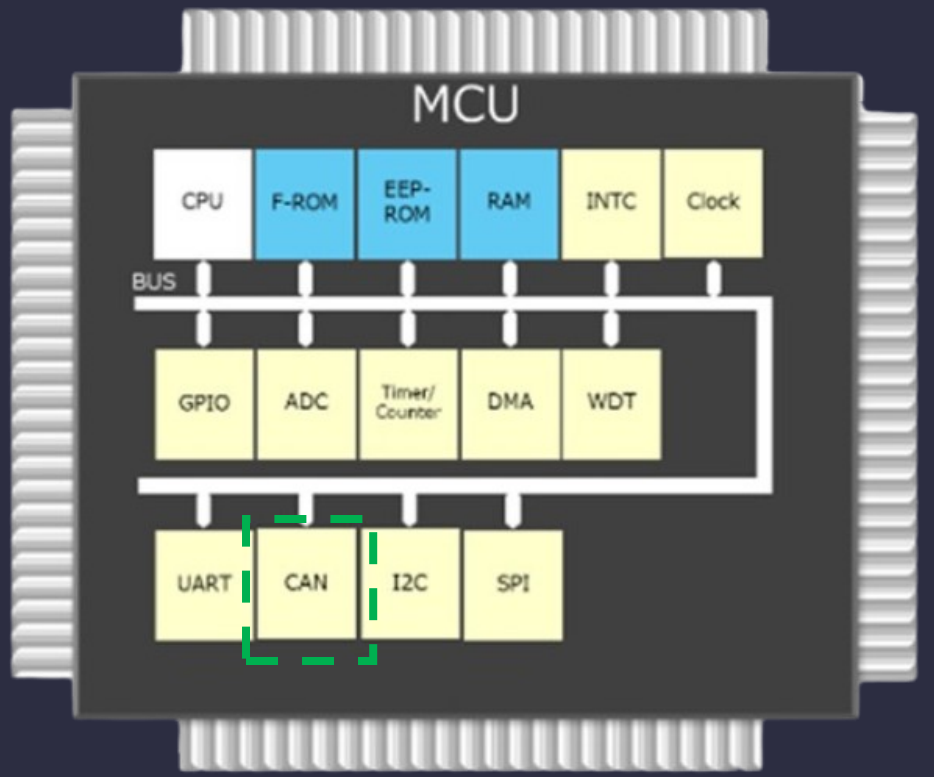


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - CAN (Control Area Network) Interface



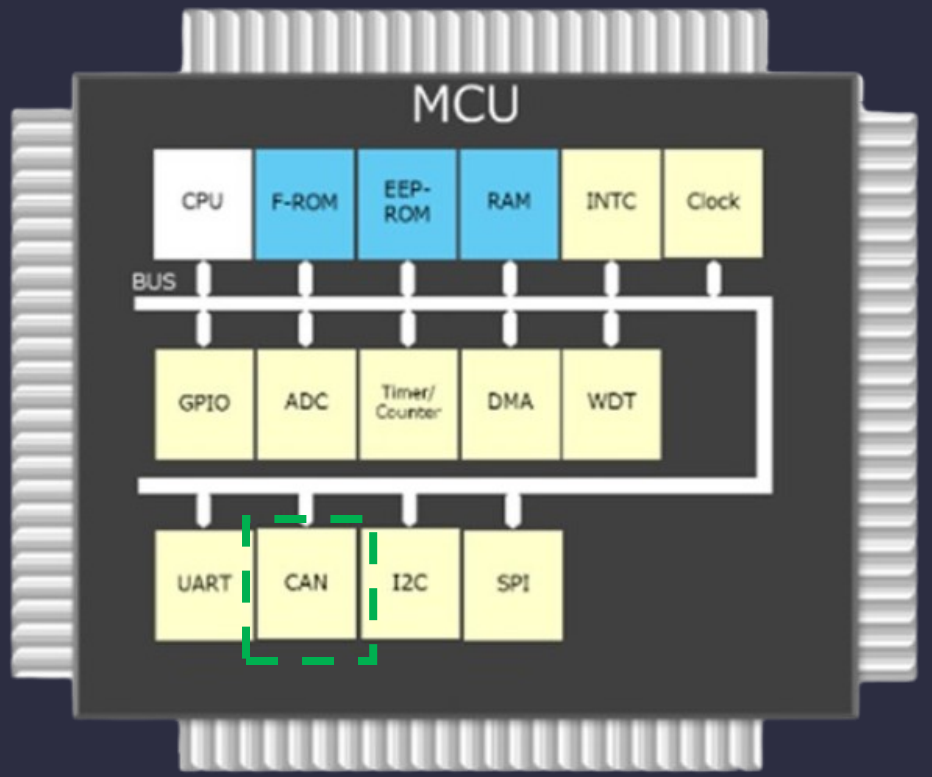


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - CAN (Control Area Network) Interface
  - Speed up to 1Mbit/s

Bit Rate	Bit time
1000 kbit/s	1 us
800 kbit/s	1.25 us
500 kbit/s	2 us
250 kbit/s	4 us
125 kbit/s	8 us
50 kbit/s	20 us
20 kbit/s	50 us

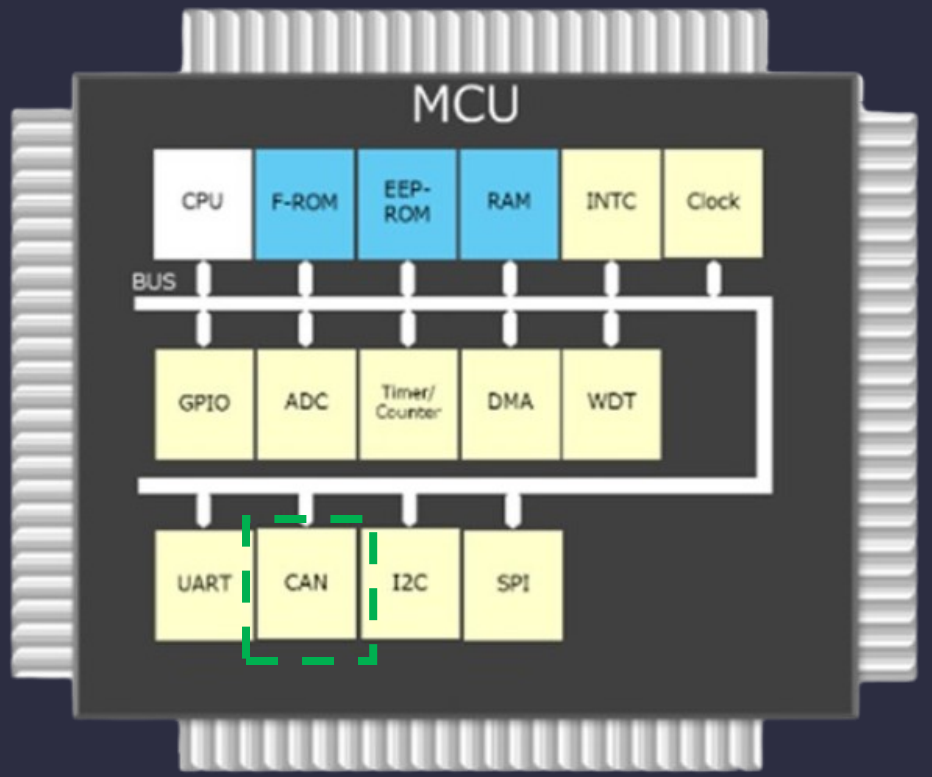


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

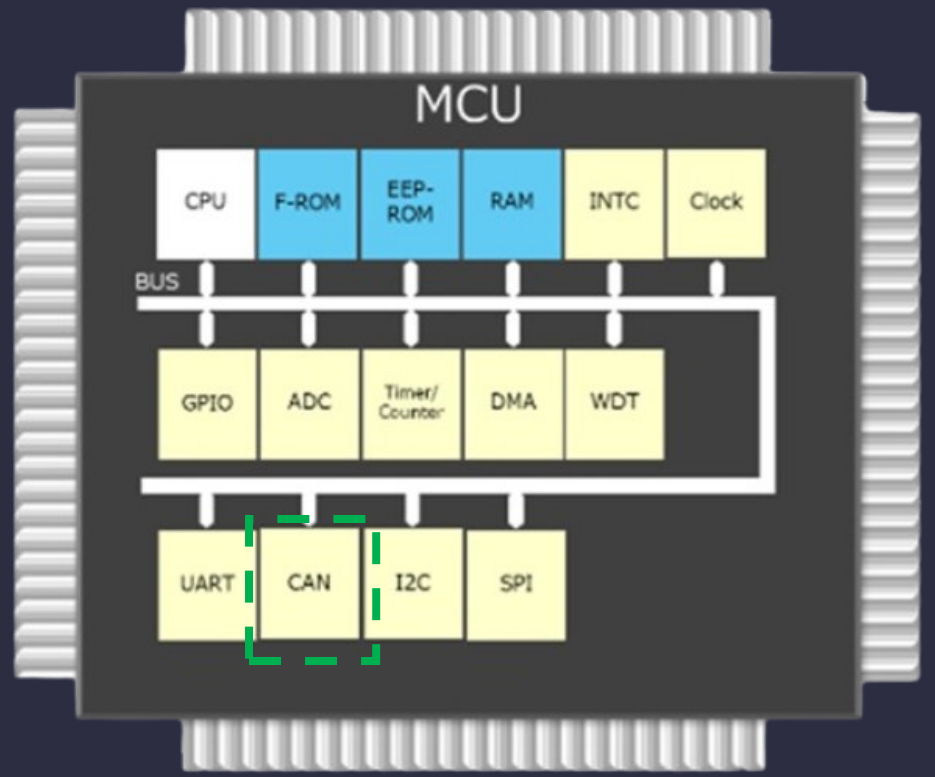
  - CAN (Control Area Network) Interface
  - CAN Messages

  - Broadcast to All Nodes!
  - Can listed all nodes
  - Maximum Payload 94 Bits
  - Packet Types
    - Data Frame
    - Remote Frame (0 Byte Data Frame)

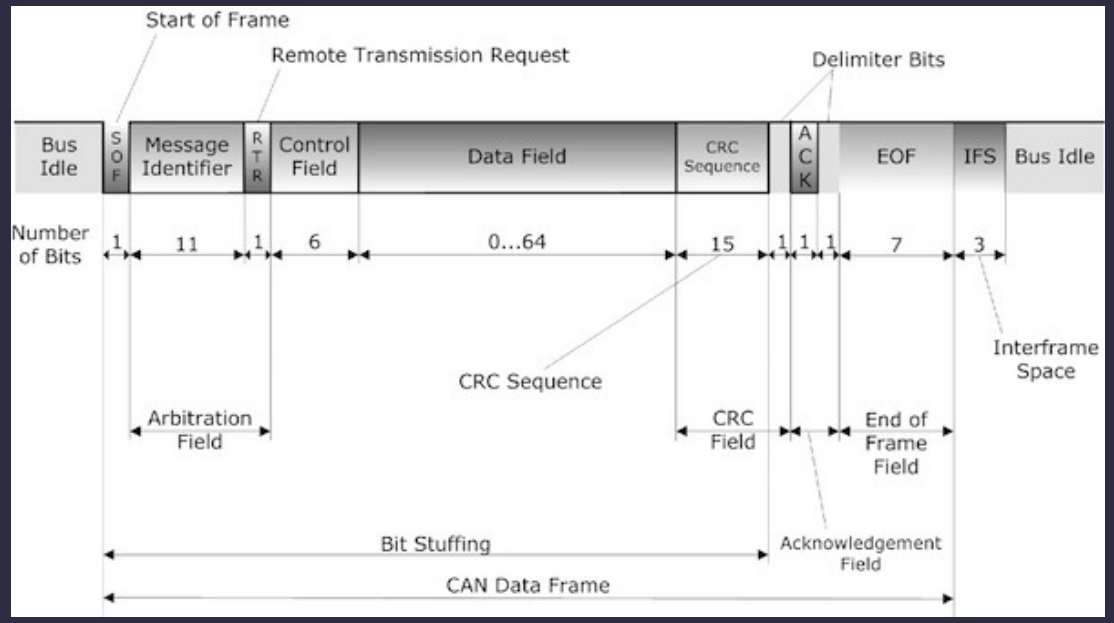


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

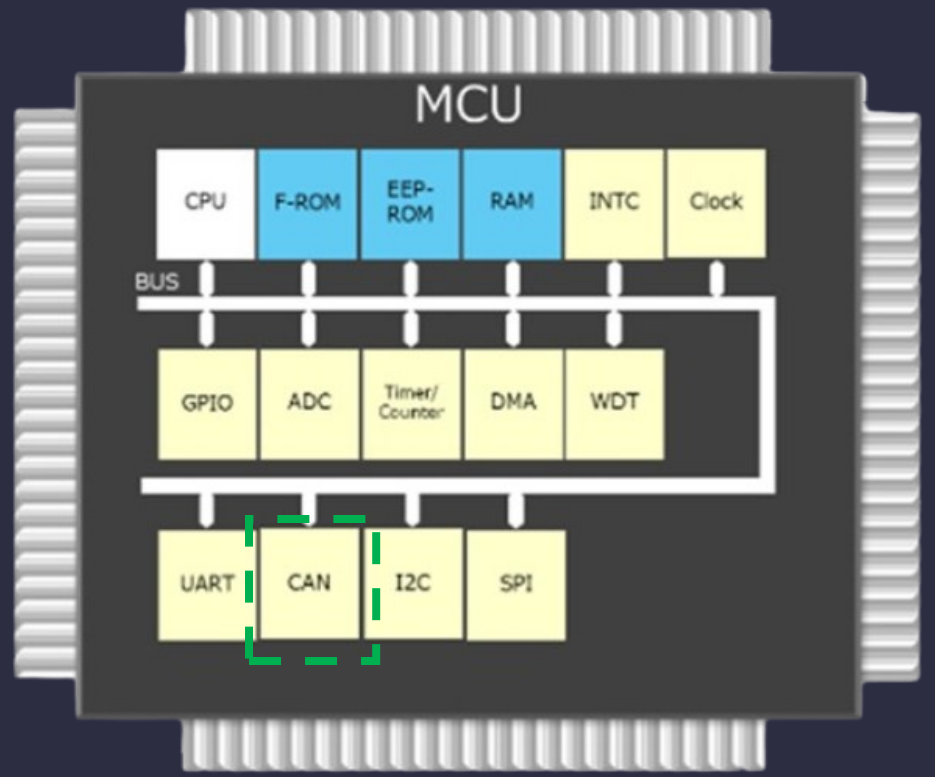


- CAN (Control Area Network) Interface
- Packet Structure
  - Data Frame
  - Remote Frame (With no data)

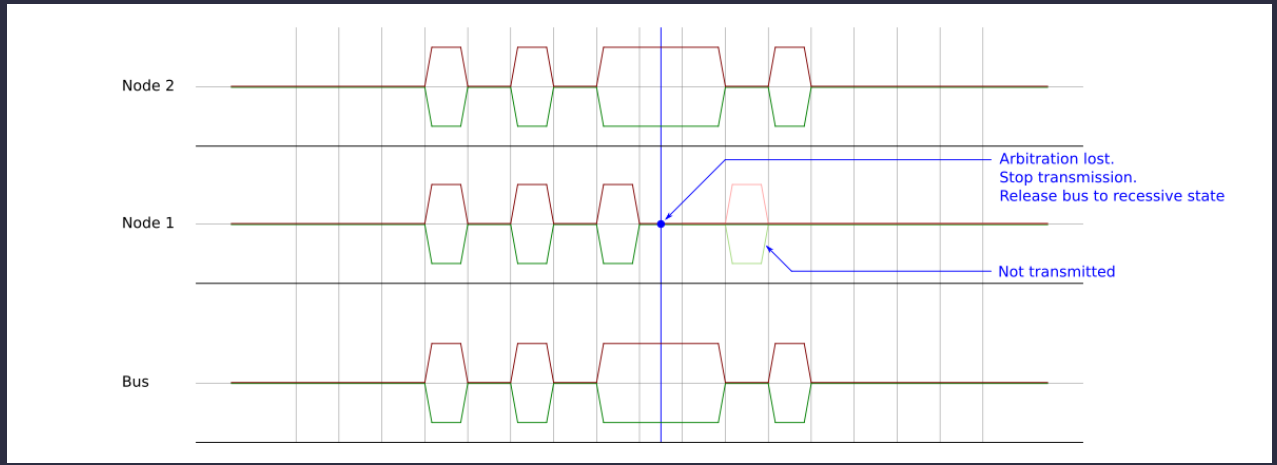


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

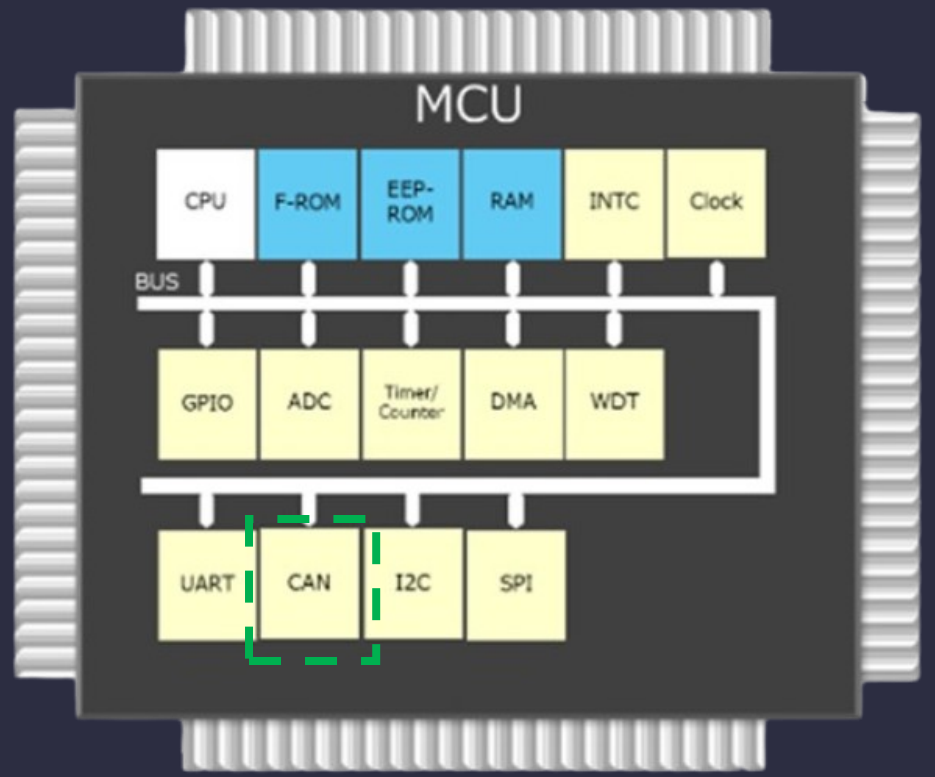


- CAN (Control Area Network) Interface
- Arbitration
- When two nodes attempt to transmit at the same time an arbitration process determines which one takes preference. While transmitting, each node reads the bus state as well. If a node detects that one of its recessive bits has been driven dominant by another node, then it stops transmitting.

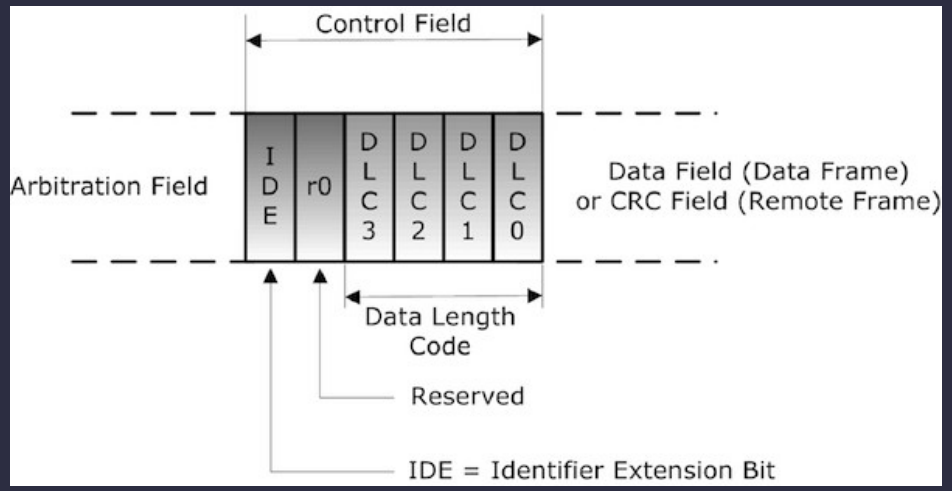


MCU & MPU Architectures, Interfaces

- Microcontroller Unit



- CAN (Control Area Network) Interface
- Control Bits

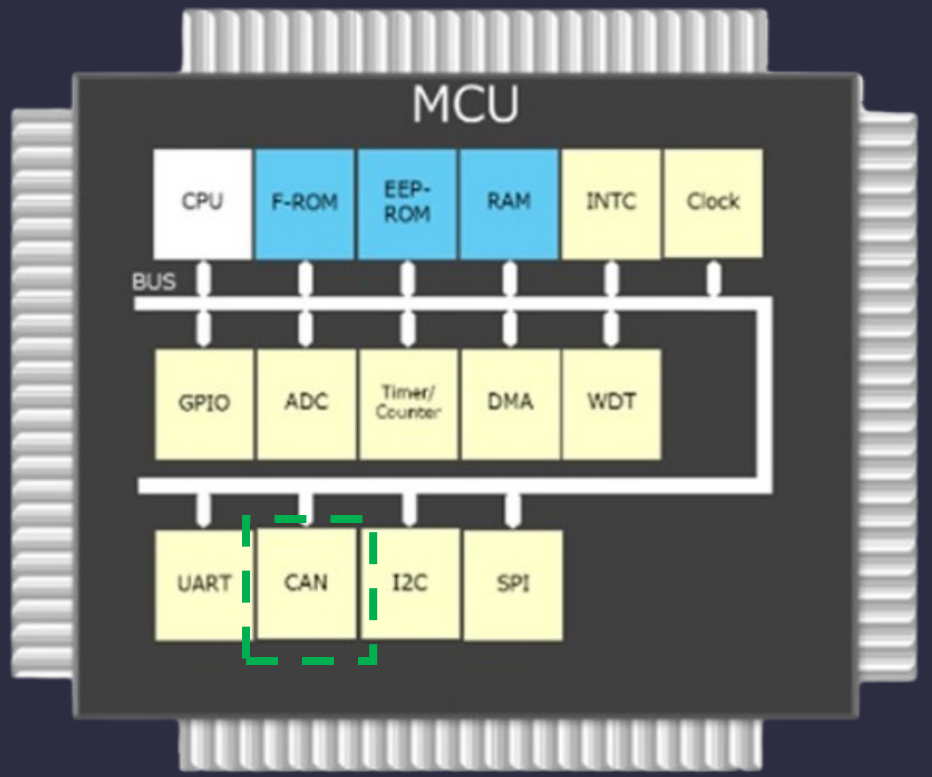


DLC (Data Length Code) usually using for indicating data length

Greater then 8 using for application specific purposes

MCU & MPU Architectures, Interfaces

- Microcontroller Unit



- CAN (Control Area Network) Interface
- CRC Calculation
- Algorithm:

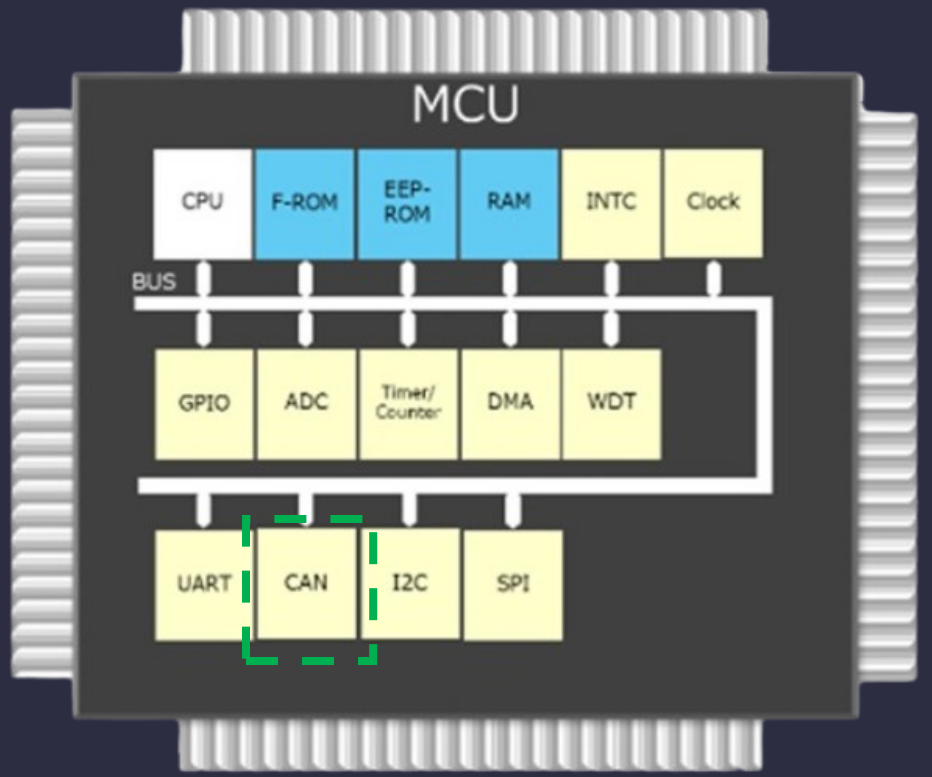
Name: CRC-16-CCITT-FALSE
Initial value: 0xFFFF
Poly: 0x1021
Reverse: no
Output XOR: 0

```
uint16_t crc16(char* pData, int length)
{
    uint8_t i;
    uint16_t wCrc = 0xffff;
    while (length--) {
        wCrc ^= *(unsigned char *)pData++ << 8;
        for (i=0; i < 8; i++)
            wCrc = wCrc & 0x8000 ? (wCrc << 1) ^ 0x1021 : wCrc << 1;
    }
    return wCrc & 0xffff;
}
```

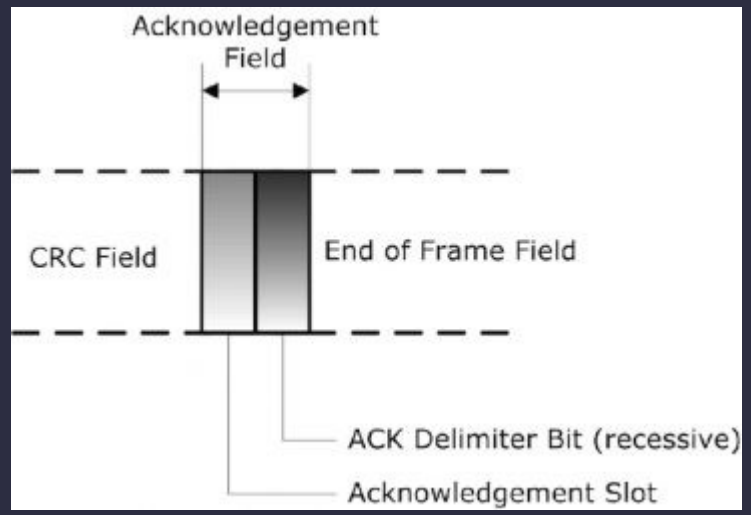
Sample C Code

MCU & MPU Architectures, Interfaces

- Microcontroller Unit



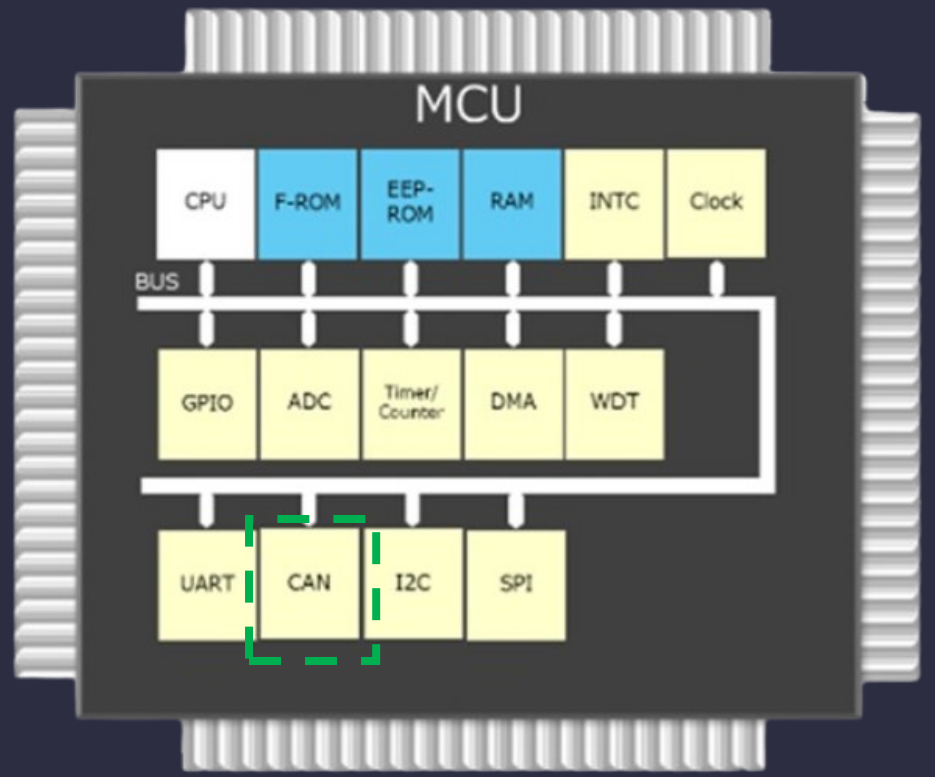
  - CAN (Control Area Network) Interface
  - Acknowledge



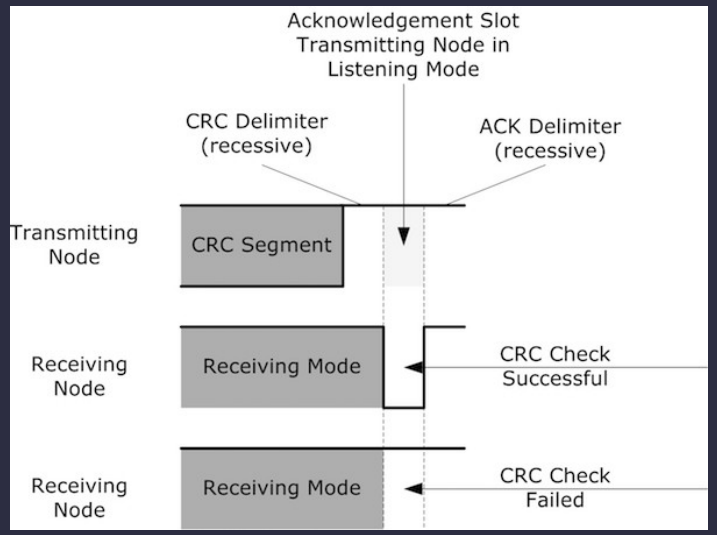
  - Succesfully received and verified CRC from receiving nodes in the network

MCU & MPU Architectures, Interfaces

- Microcontroller Unit



- CAN (Control Area Network) Interface
- Acknowledge



- Succesfully received and verified CRC from receiving nodes in the network

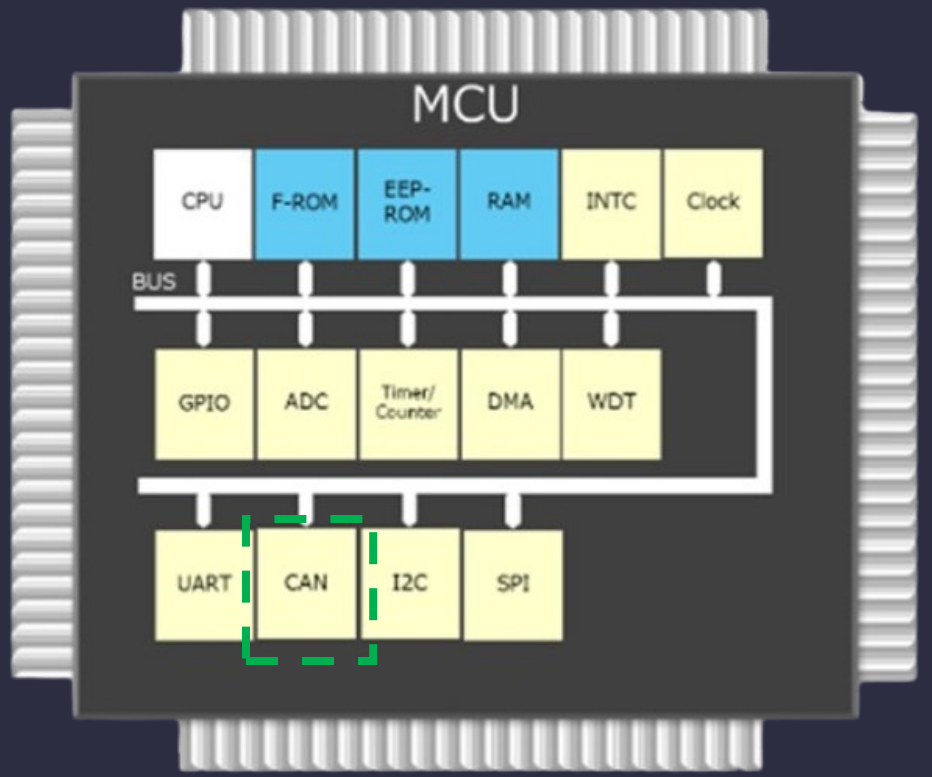
MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - CAN (Control Area Network) Interface
  - Acknowledge

  - If all nodes in the network determine a checksum error, meaning the sending node monitors a recessive level in the ACK slot, it is clear that the sending node calculated a wrong checksum. The error is therefore local at the sending node.

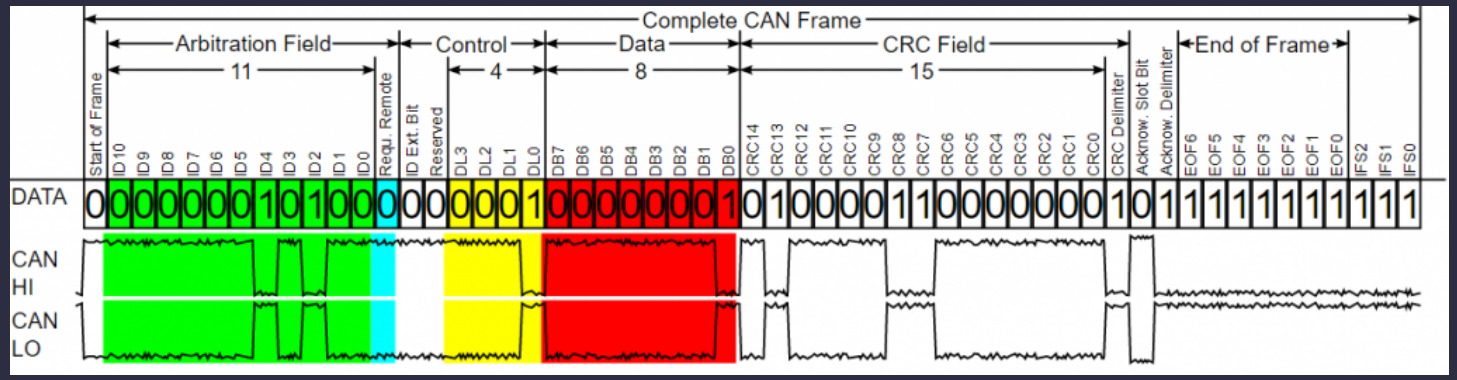
  - The CAN standard allows the so-called “self-retirement” (or self-removal) of nodes from the network due to an excessive number of transmit or receive errors

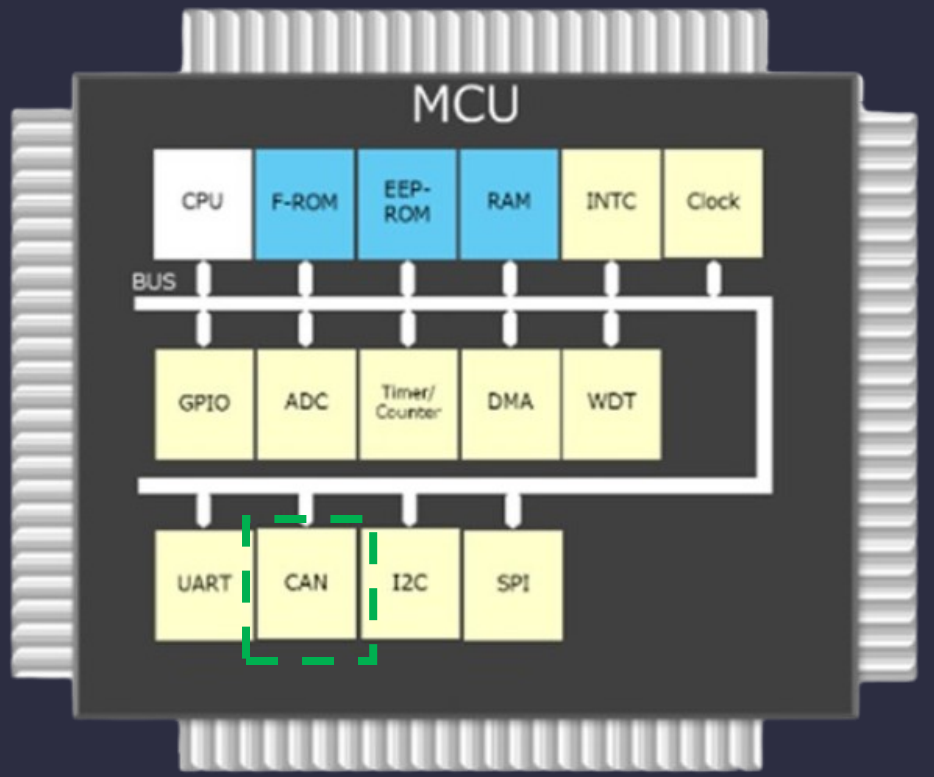


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - CAN (Control Area Network) Interface
  - Example



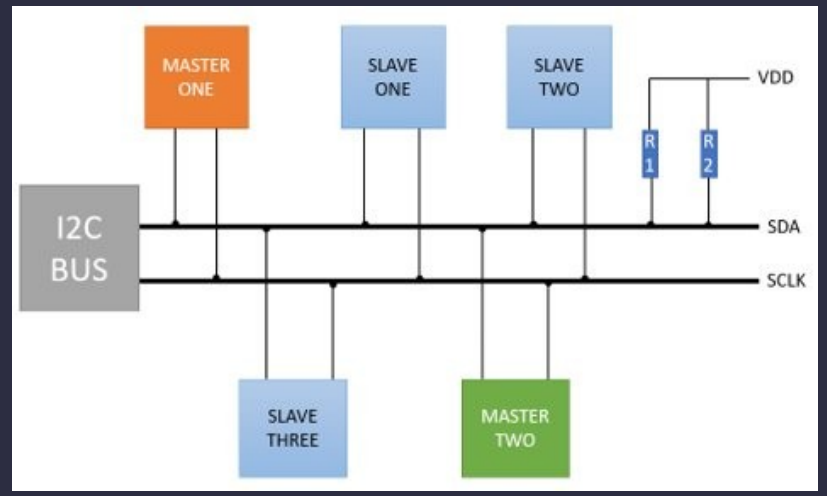


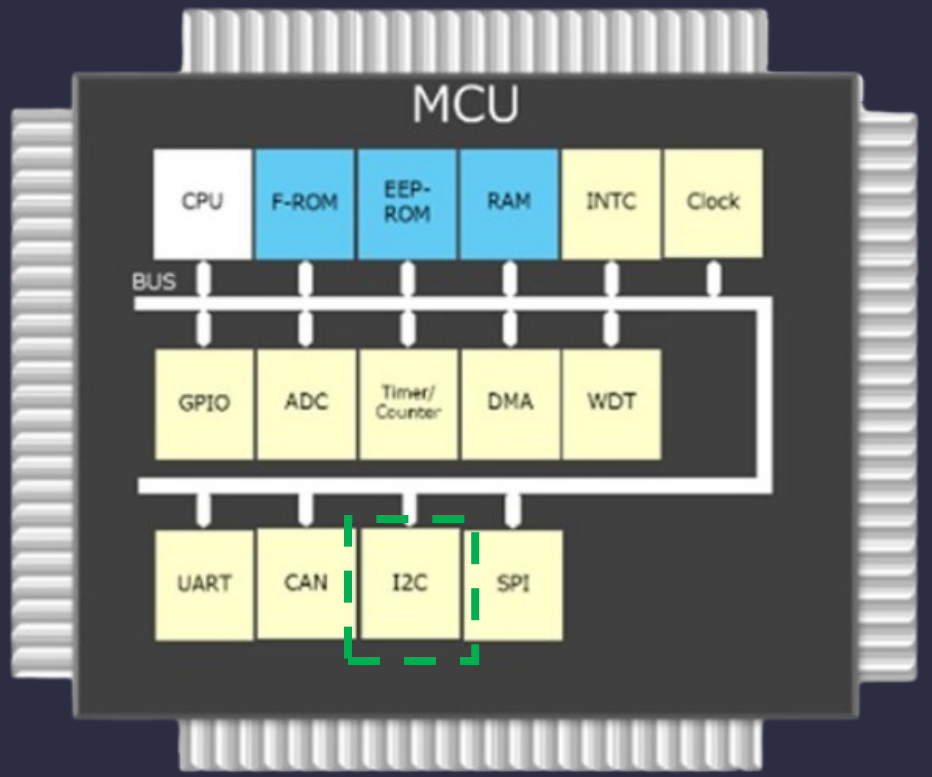
MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - I2C – Two Wire
  - Defined by Philips, 1982
  - Last Update 2007
  - Usual Speeds:
    - 100KHz
    - 400KHz

  - SCK: Clock
  - SDA: Data

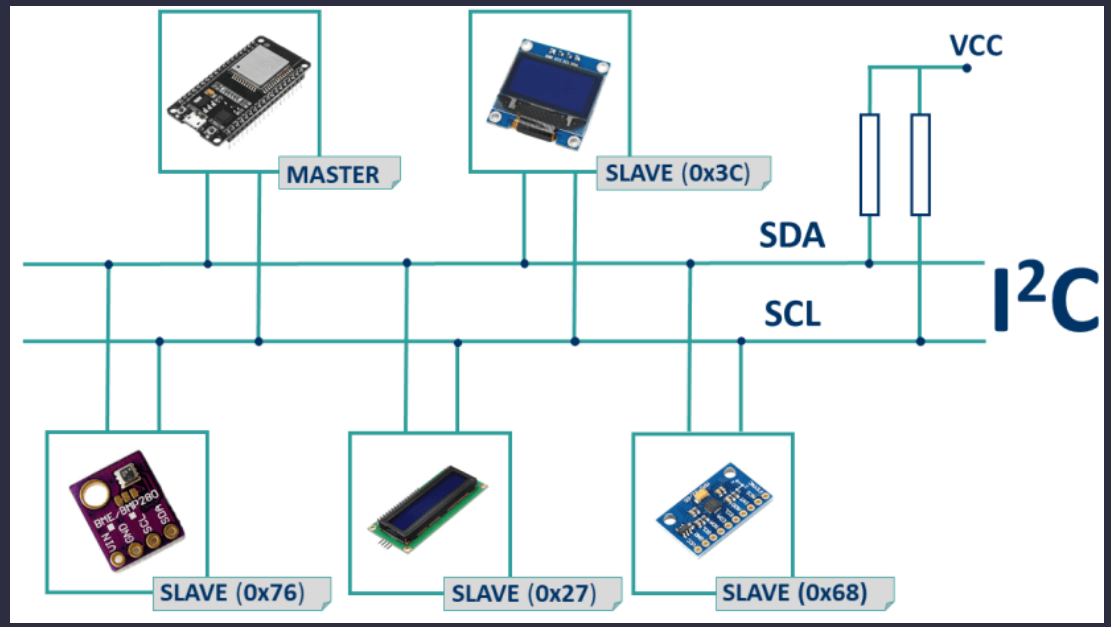


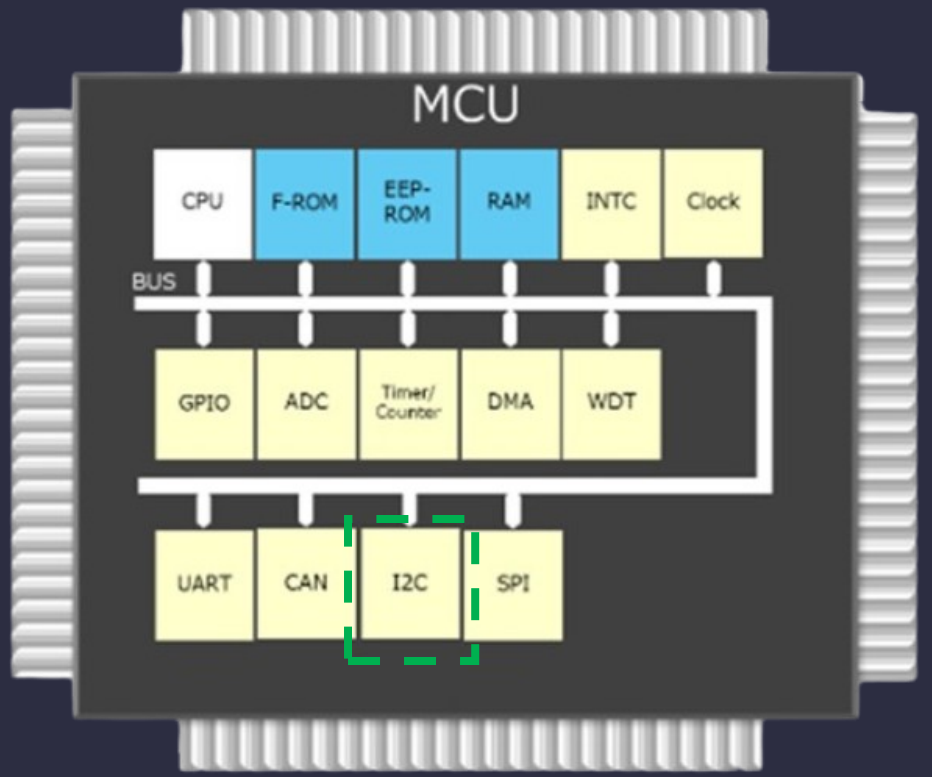


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - I2C – Two Wire

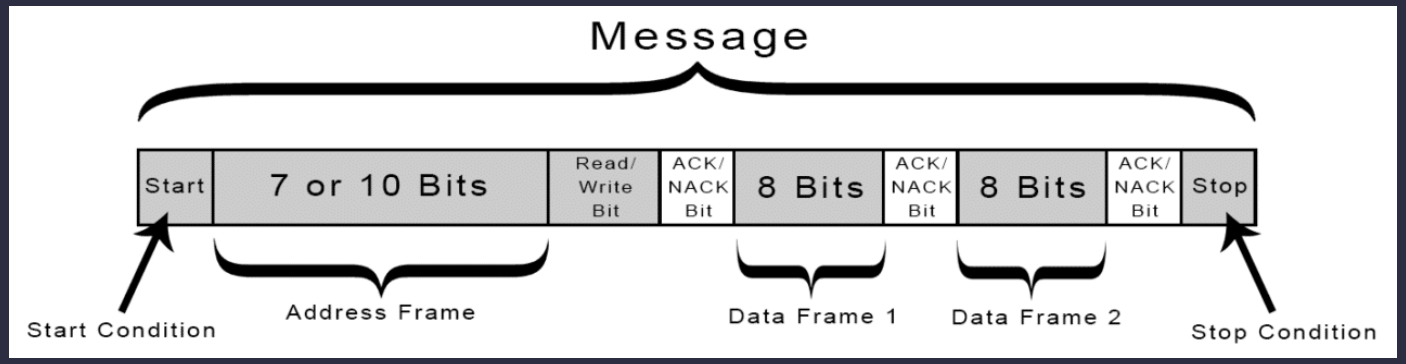


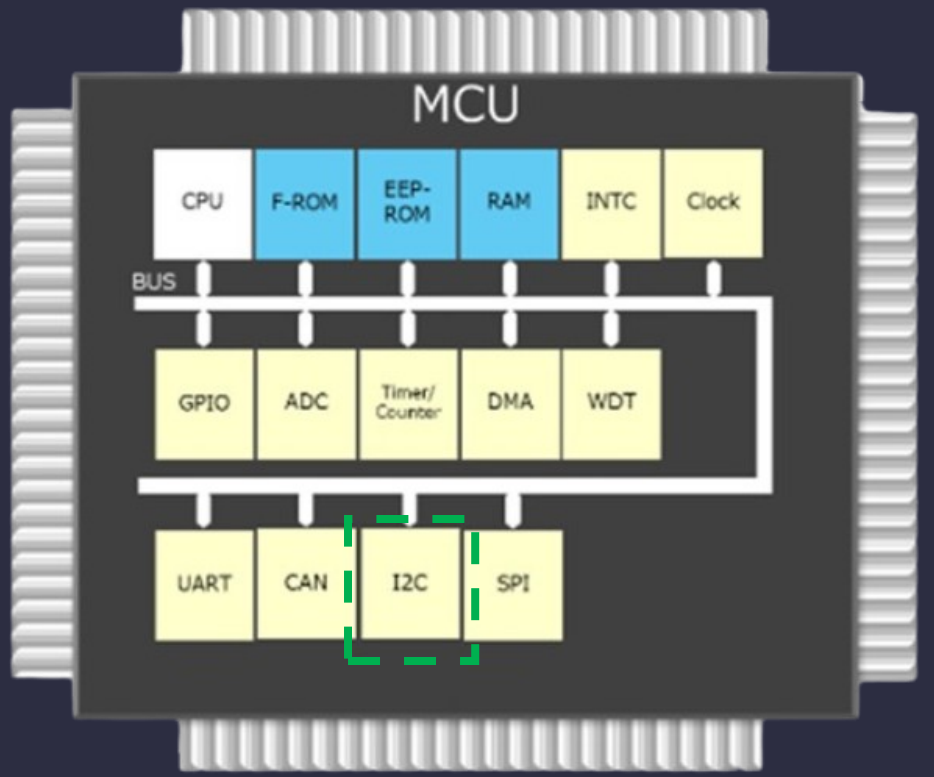


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - I2C – Two Wire
  - Read 1, Write 0
  - ACK 0, NACK 1
  - Start 0

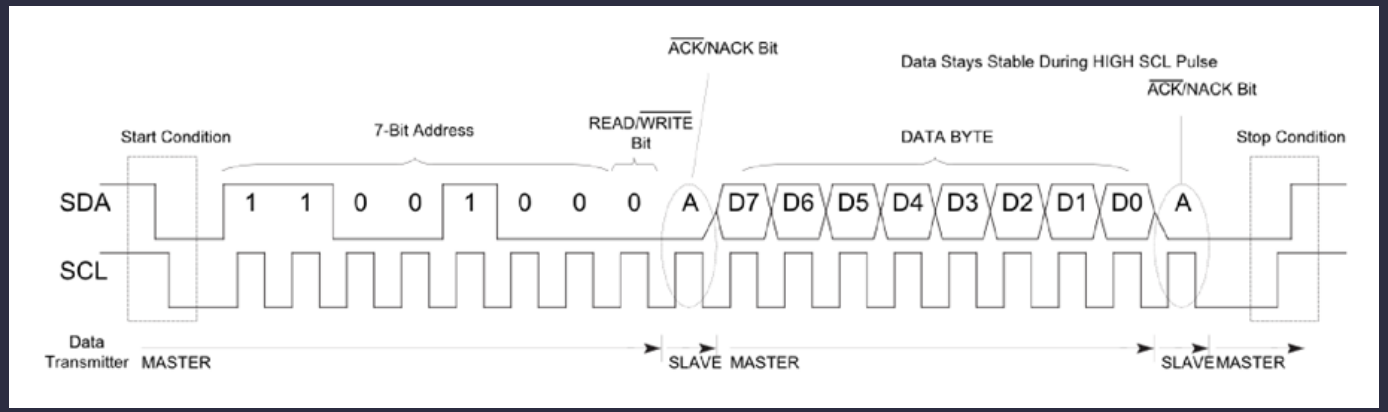


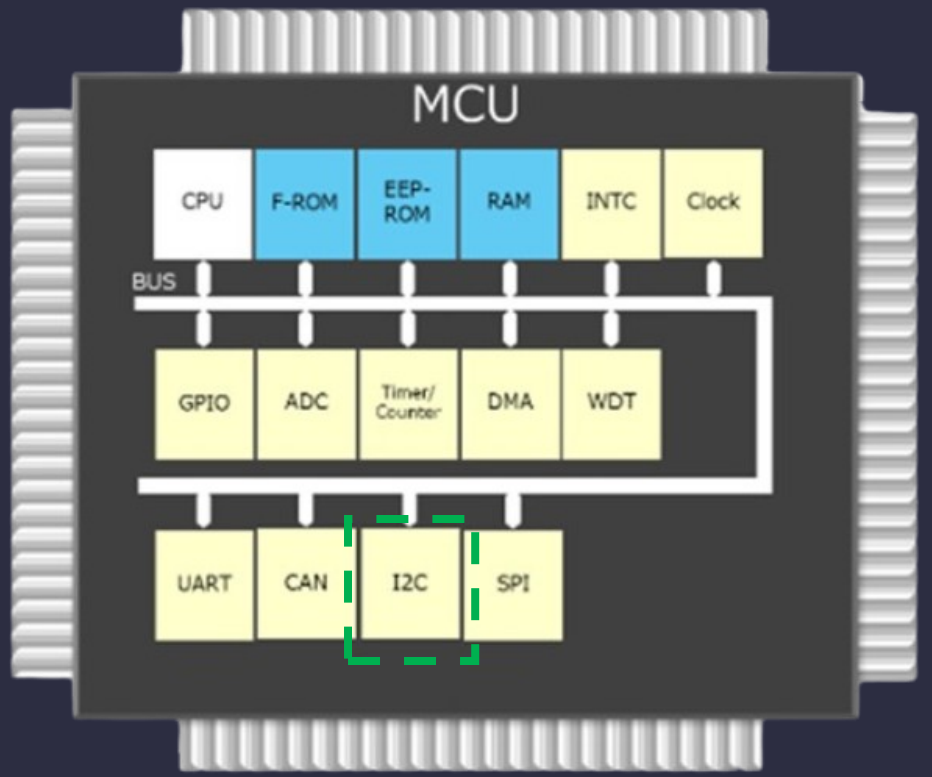


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - I2C – Two Wire
  - Simple Write Example

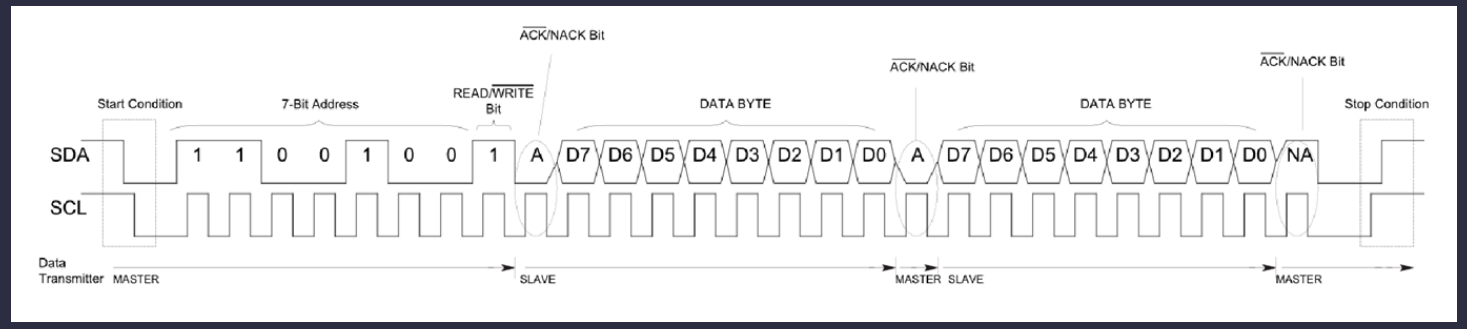


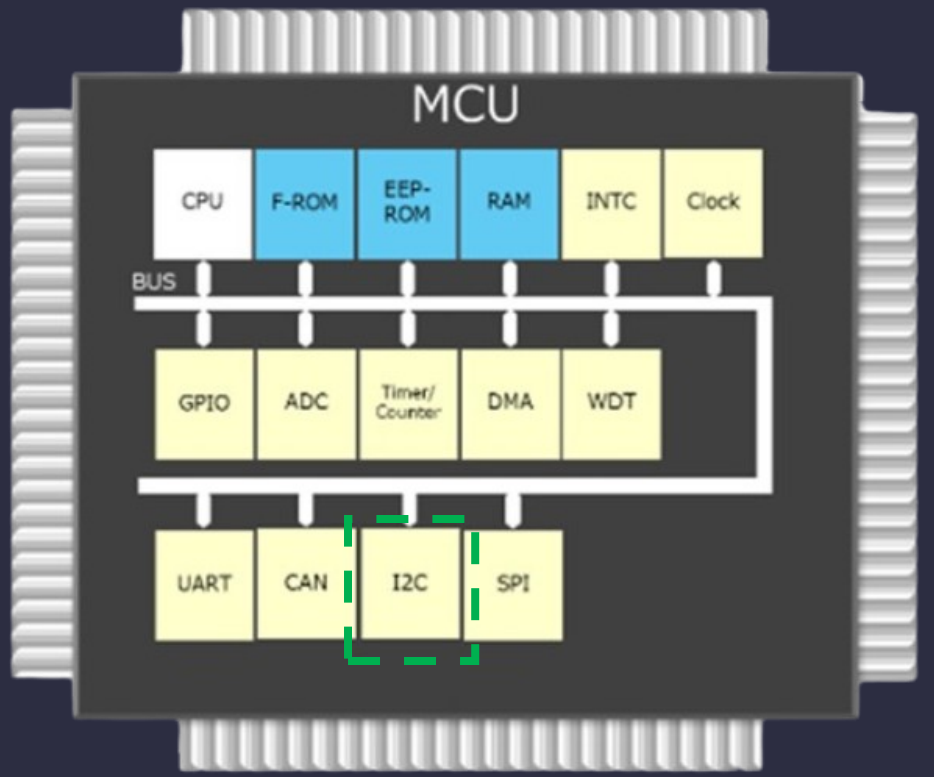


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - I2C – Two Wire
  - Simple Read Example



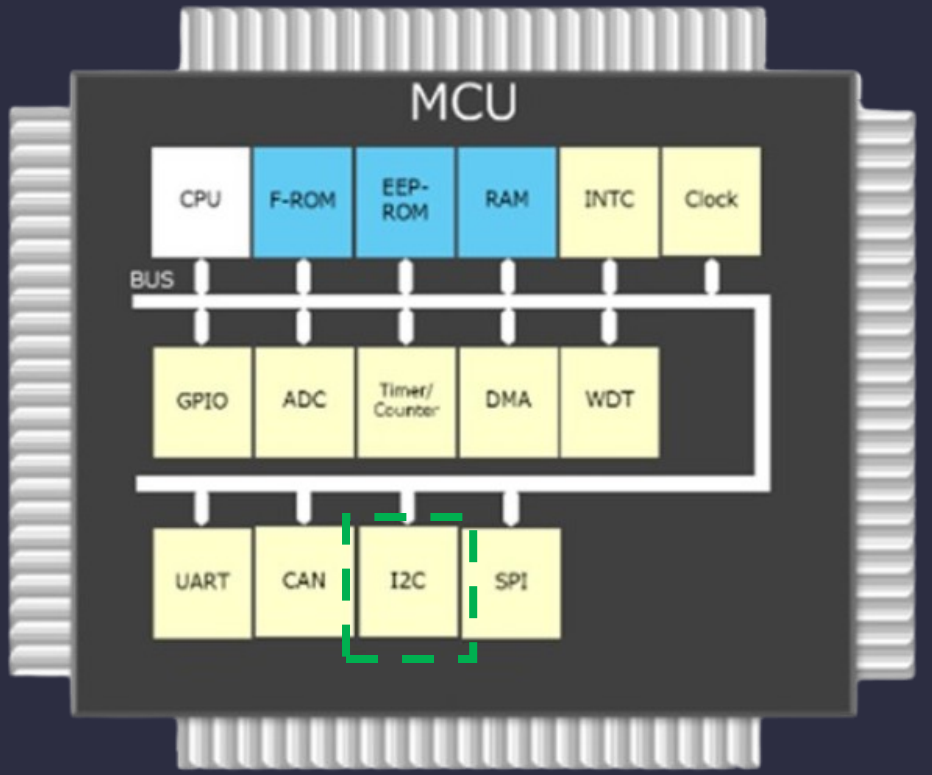


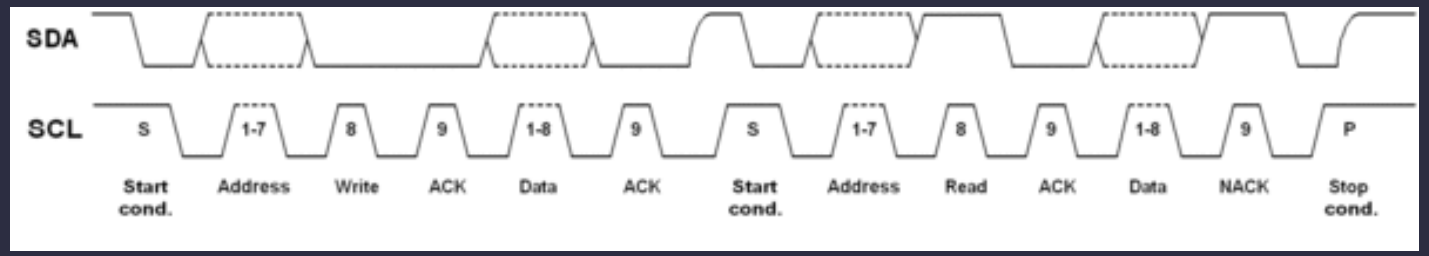
MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - I2C – Two Wire
  - Repeated Start

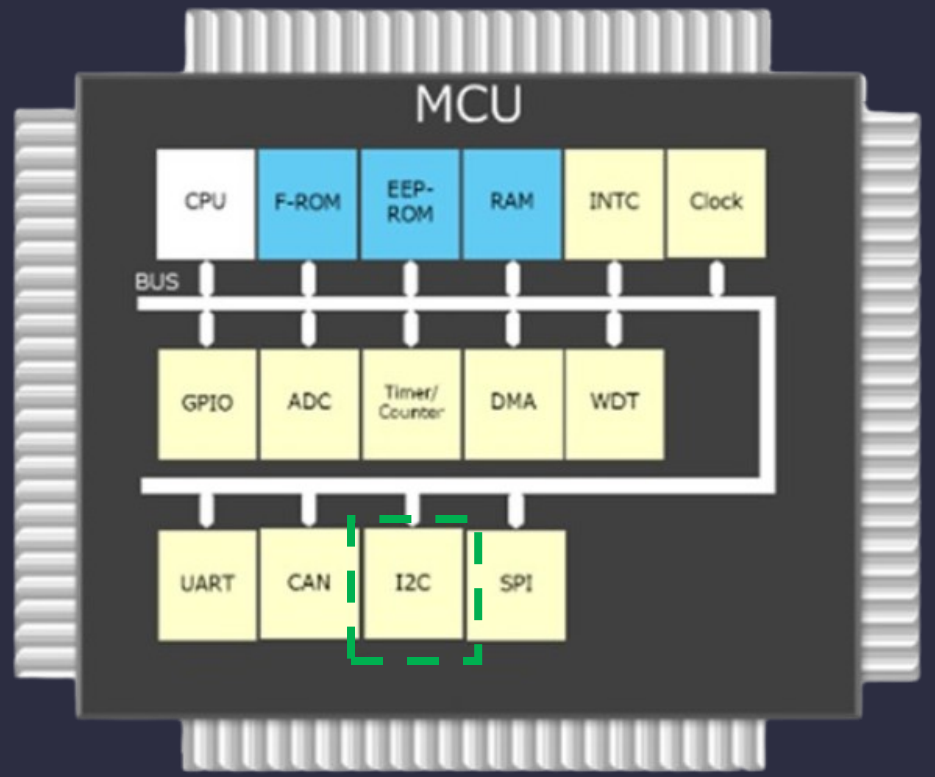
  - Sometimes the master needs to perform multiple message exchanges in one communication such as transferring messages with different slaves, or switching read and write operations, and does not want to be interfered with by other master during this period, then you can use the ‘repeat start condition’



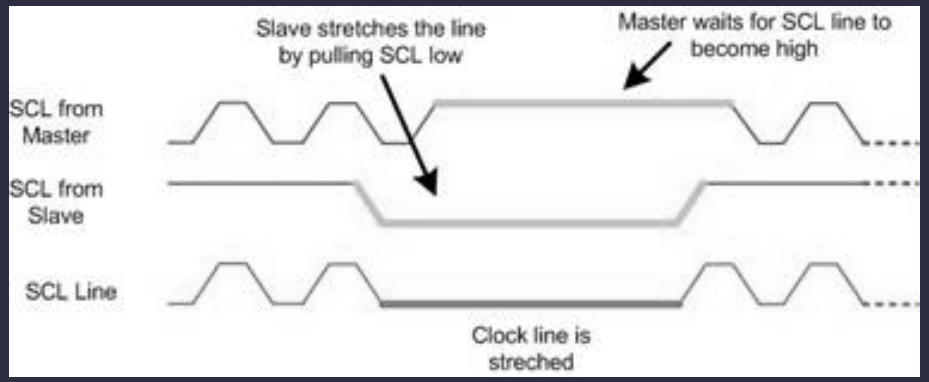


MCU & MPU Architectures, Interfaces

- Microcontroller Unit



  - I2C – Two Wire
  - Clock Streching
  - In the master-Slave communication process of I2C, the SCL clock on the bus is always generated and controlled by the master, but if the slave cannot keep up with the speed of the master, the I2C protocol stipulates that the slave can pull down the SCL clock line.

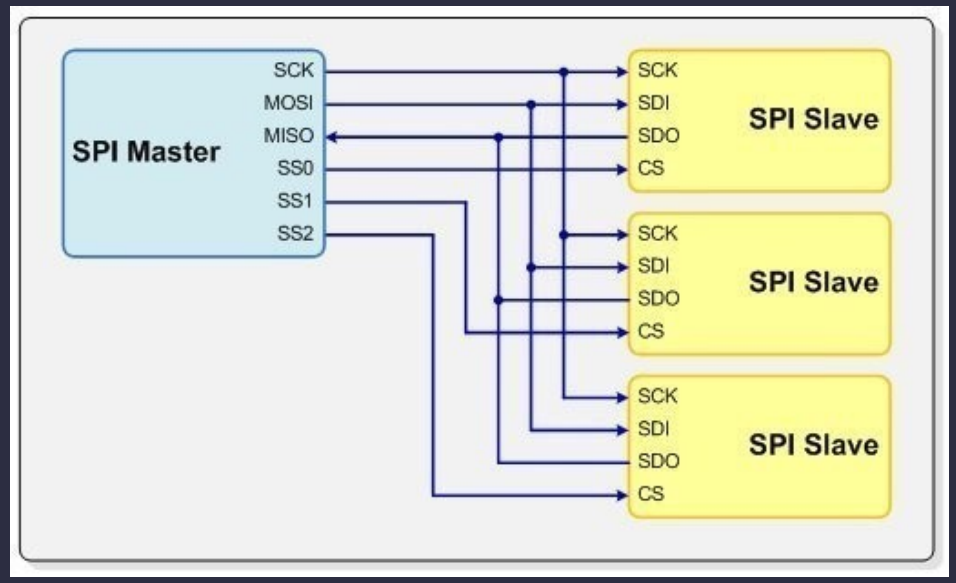


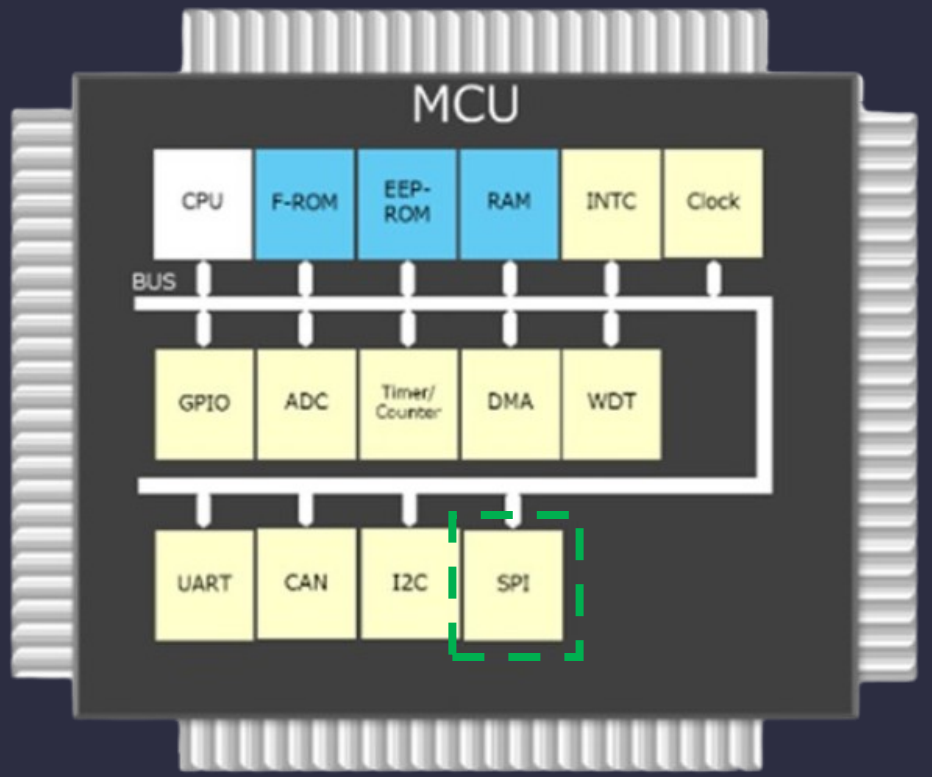
  - Defined device specific

MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - SPI (Serial Peripheral Interface)
  - Inveted by Motorola, 1980
  - Last update on 2000
  - Generally Max Freq 25 MHz

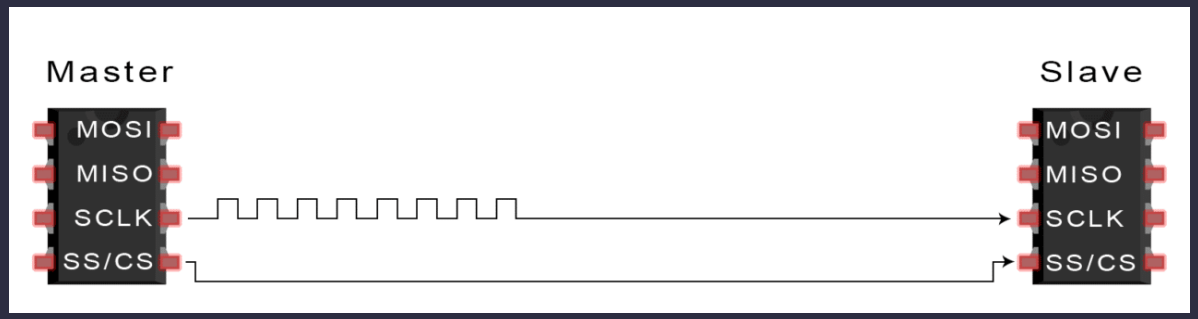


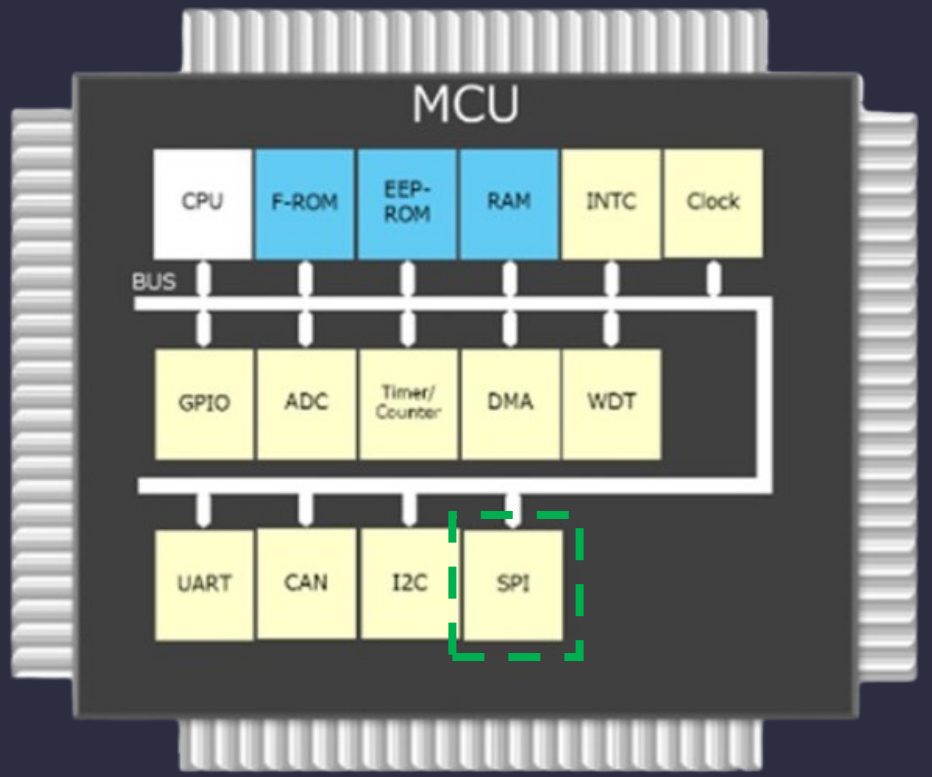


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - SPI (Serial Peripheral Interface)
  - Transmission
    Slave Select

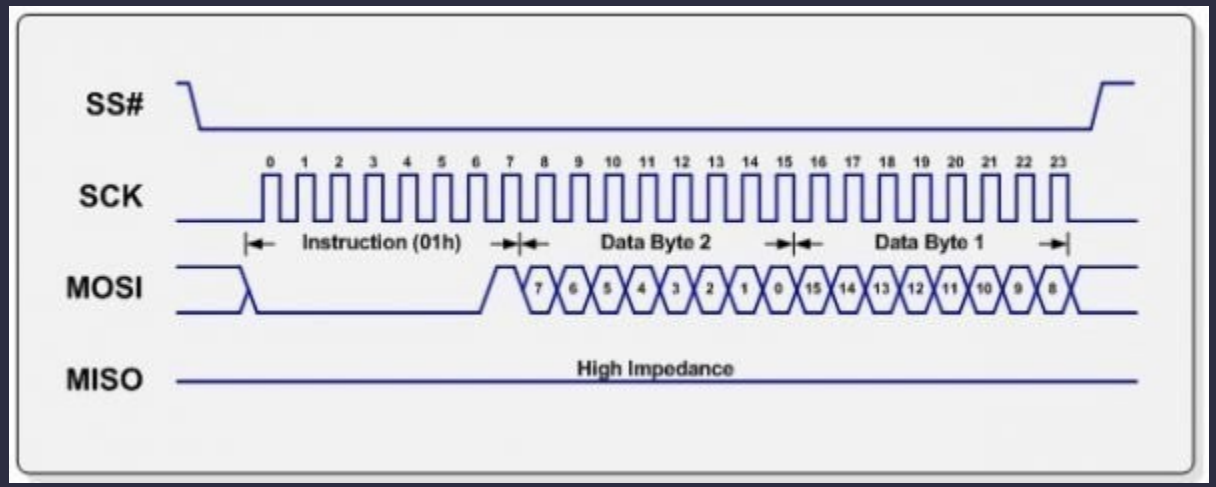


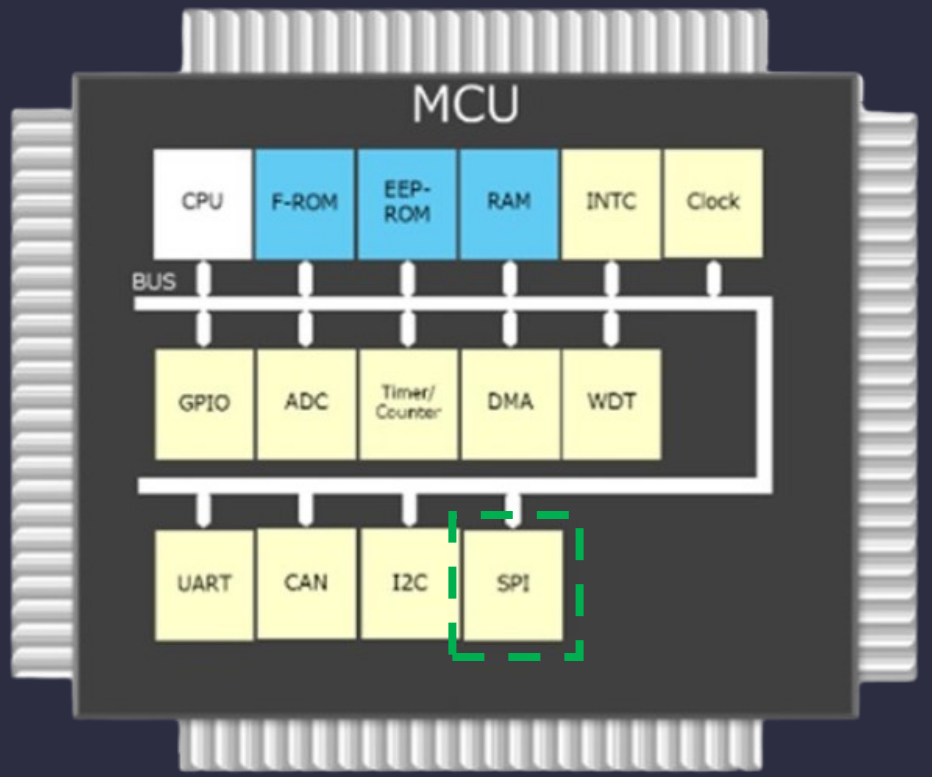


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - SPI (Serial Peripheral Interface)
  - Modes
  - Simple Write

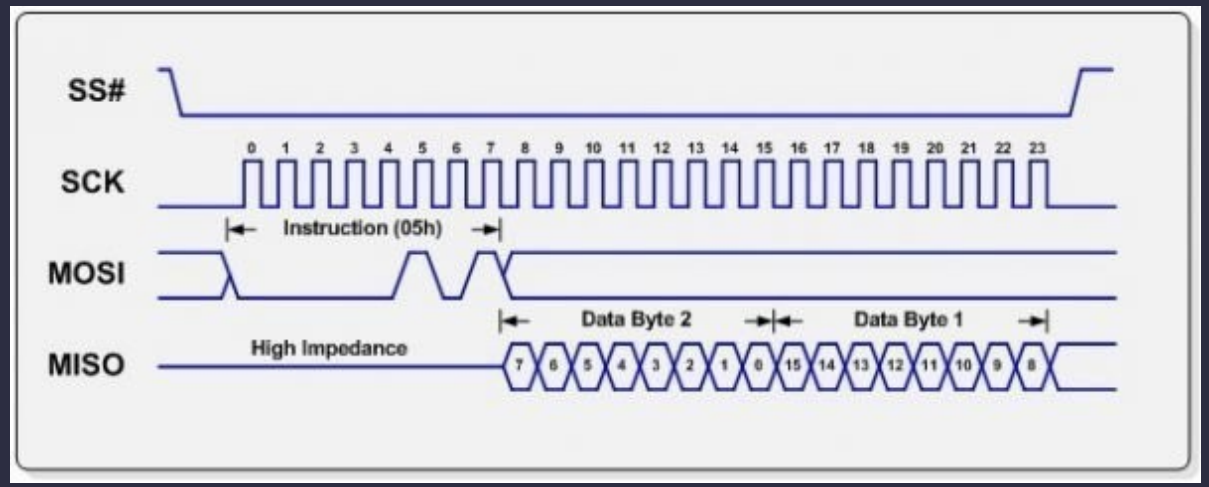


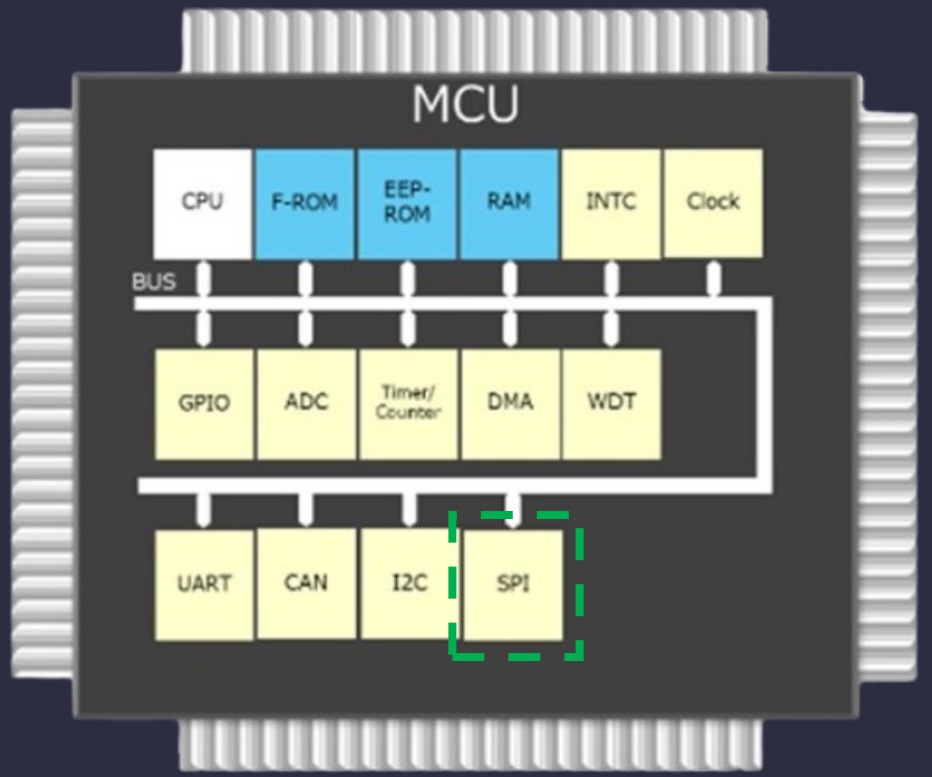


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

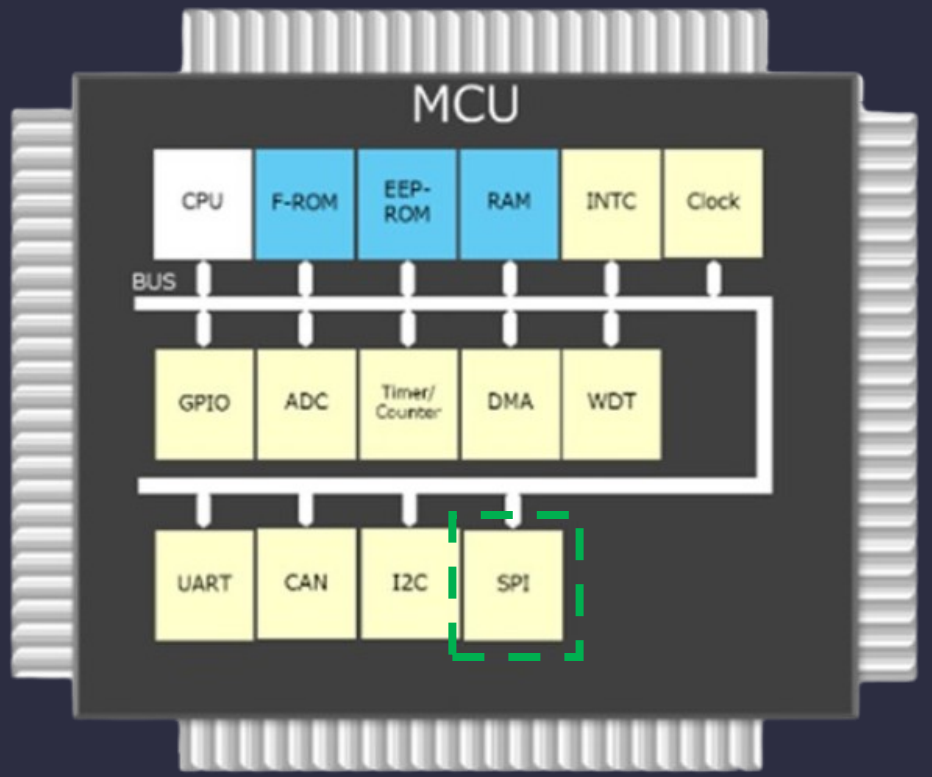
  - SPI (Serial Peripheral Interface)
  - Modes
  - Simple Read



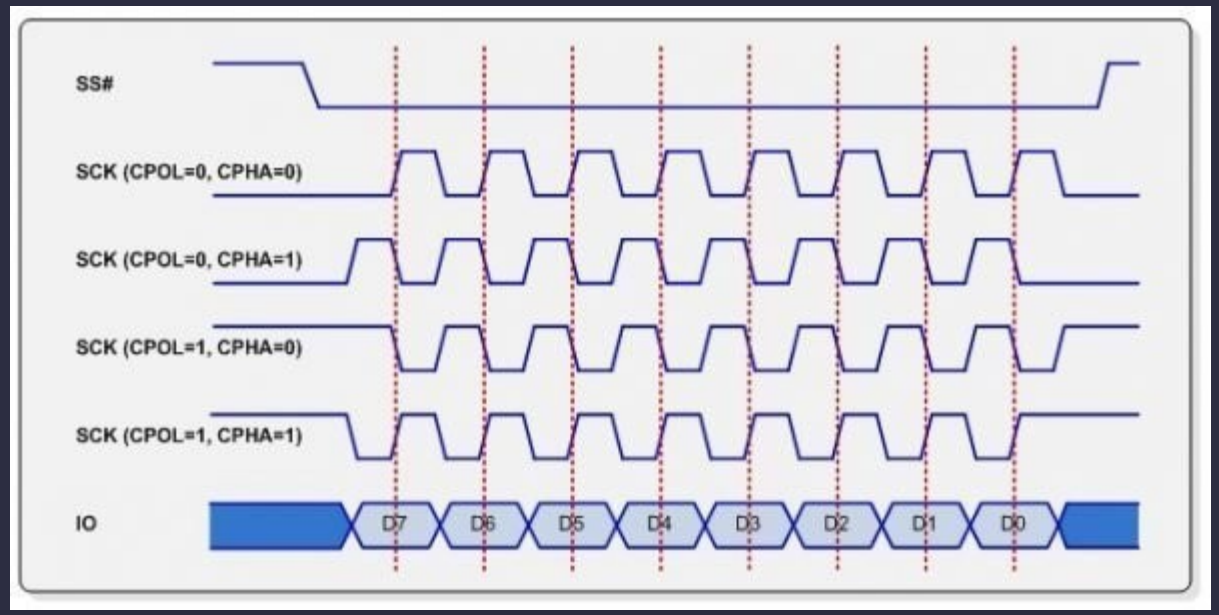


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

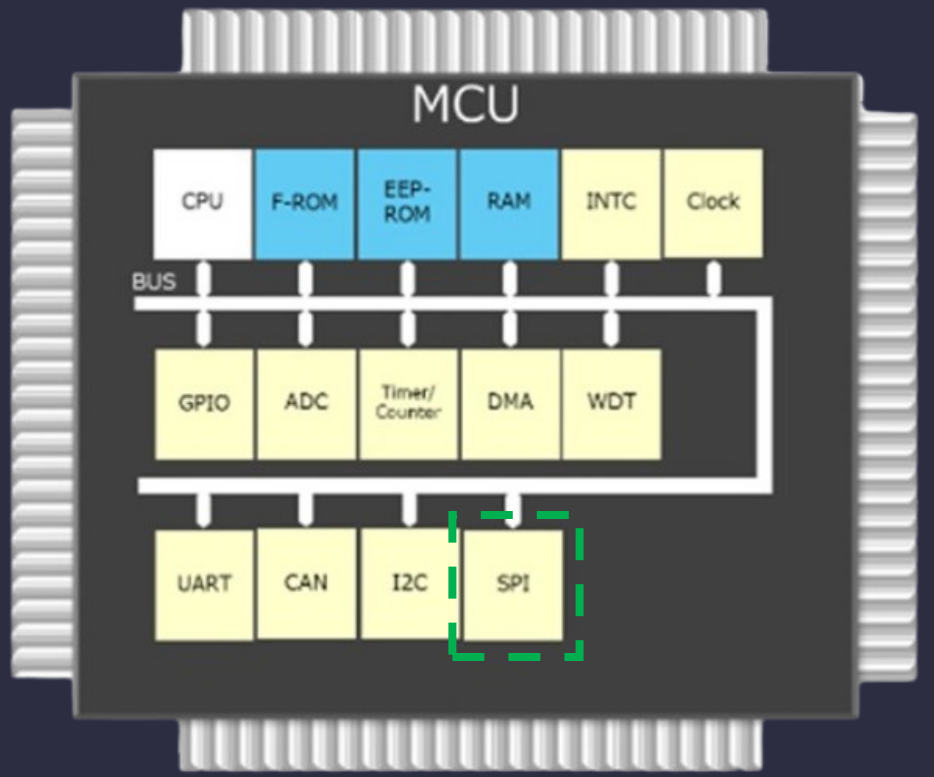


- SPI (Serial Peripheral Interface)
- Modes
- CPOL (Clock Polarity), CPHA (Clock Phase)

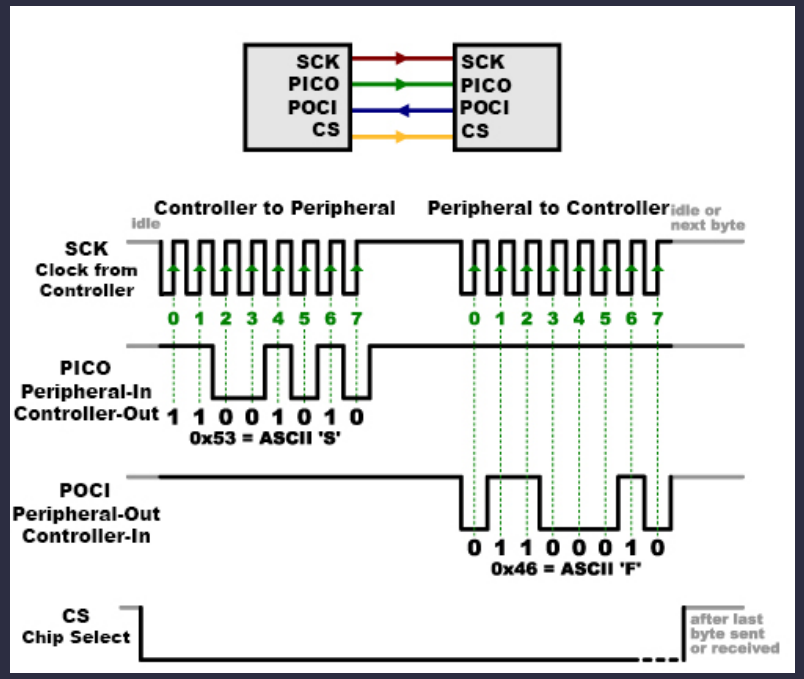


MCU & MPU Architectures, Interfaces

- Microcontroller Unit



  - SPI (Serial Peripheral Interface)
  - Transmission



MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - Use Cases
    - Atmega2560, Microchip Technology
    - Datasheet: https://ww1.microchip.com/downloads/en/devicedoc/atmel-2549-8-bit-avr-microcontroller-atmega640-1280-1281-2560-2561_datasheet.pdf

Atmel ATmega640/V-1280/V-1281/V-2560/V-2561/V

8-bit Atmel Microcontroller with 16/32/64KB In-System Programmable Flash

DATASHEET

Features

- High Performance, Low Power Atmel® AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 135 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16MHz
  - On-Chip 2-cycle Multiplier
- High Endurance Non-volatile Memory Segments
  - 64K/128K/256KBytes of In-System Self-Programmable Flash
  - 4Kbytes EEPROM
  - 8Kbytes Internal SRAM
  - Write/Erase Cycles:10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/ 100 years at 25°C
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Programming Lock for Software Security
    - Endurance: Up to 64Kbytes Optional External Memory Space
- Atmel® QTouch® library support
  - Capacitive touch buttons, sliders and wheels
  - QTouch and QMatrix acquisition
  - Up to 64 sense channels
- JTAG (IEEE® std. 1149.1 compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  - Four 16-bit Timer/Counter with Separate Prescaler, Compare- and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four 8-bit PWM Channels
  - Six/Twelve PWM Channels with Programmable Resolution from 2 to 16 Bits (ATmega1281/2561, ATmega640/1280/2560)
  - Output Compare Modulator
  - 8/16-channel, 10-bit ADC (ATmega1281/2561, ATmega640/1280/2560)
  - Two/Four Programmable Serial USART (ATmega1281/2561, ATmega640/1280/2560)
  - Master/Slave SPI Serial Interface
  - Byte Oriented 2-wire Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and Packages
  - 54/86 Programmable I/O Lines (ATmega1281/2561, ATmega640/1280/2560)
  - 64-pad QFN/MLF, 64-lead TQFP (ATmega1281/2561)
  - 100-lead TQFP, 100-ball CBGA (ATmega640/1280/2560)
  - RoHS/Fully Green
- Temperature Range:
  - -40°C to 85°C Industrial
- Ultra-Low Power Consumption
  - Active Mode: 1MHz, 1.8V: 500µA
  - Power-down Mode: 0.1µA at 1.8V
- Speed Grade:
  - ATmega640V/ATmega1280V/ATmega1281V:
    - 0 - 8MHz @ 1.8V - 5.5V, 0 - 8MHz @ 2.7V - 5.5V
  - ATmega2560V/ATmega2561V:
    - 0 - 2MHz @ 1.8V - 5.5V, 0 - 8MHz @ 2.7V - 5.5V
  - ATmega640/ATmega1280/ATmega1281:
    - 0 - 8MHz @ 2.7V - 5.5V, 0 - 16MHz @ 4.5V - 5.5V
  - ATmega2560/ATmega2561:
    - 0 - 16MHz @ 4.5V - 5.5V

2549Q–AVR–02/2014

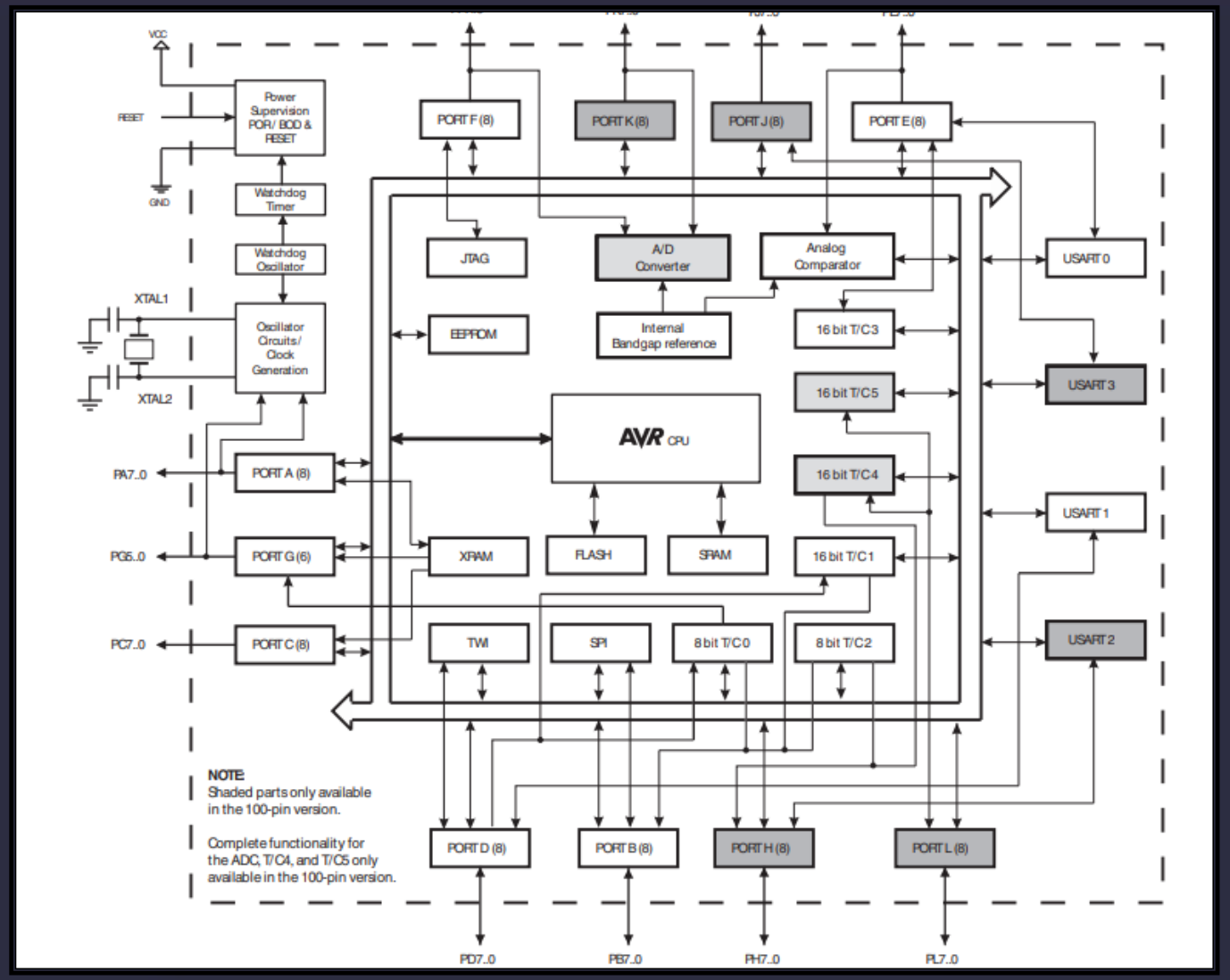
Atmega 2560 Datasheet, 465 Pages!

MCU & MPU Architectures, Interfaces

- Microcontroller Unit
  - Atmega2560 Architecture
  - Top Level View
    - 8 Bit Microcontroller
    - Single Cycle Instructions
    - 32x32bit General Purpose Registers
    - Memories

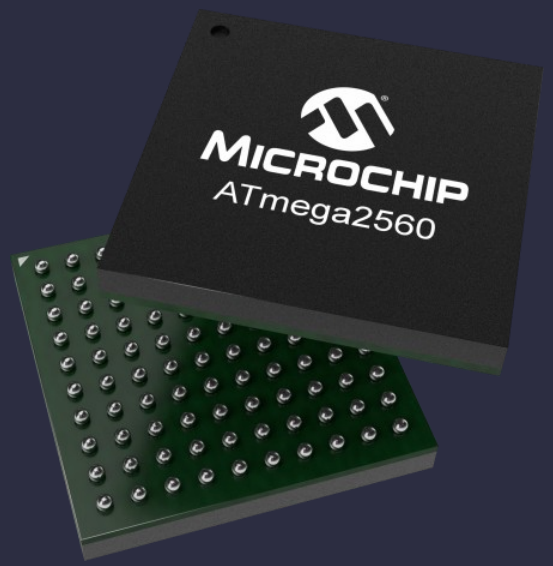
Table. Configuration Summary

Device	Flash	EEPROM	RAM	General Purpose I/O pins	16 bits resolution PWM channels	Serial USARTs	ADC Channels
ATmega640	64KB	4KB	8KB	86	12	4	16
ATmega1280	128KB	4KB	8KB	86	12	4	16
ATmega1281	128KB	4KB	8KB	54	6	2	8
ATmega2560	256KB	4KB	8KB	86	12	4	16
ATmega2561	256KB	4KB	8KB	54	6	2	8



MCU & MPU Architectures, Interfaces

- Microcontroller Unit
  - Atmega2560 Architecture
  - Top Level View
    - CBGA Package Chip



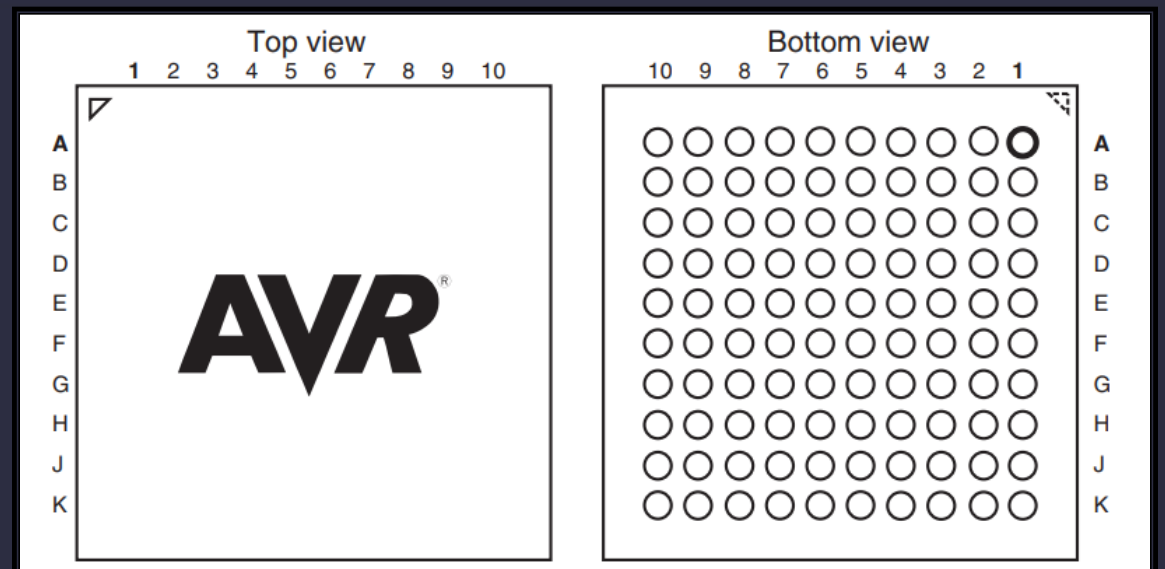
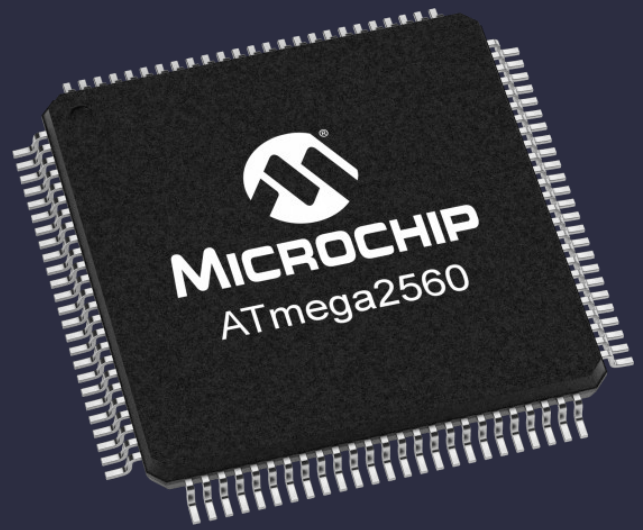


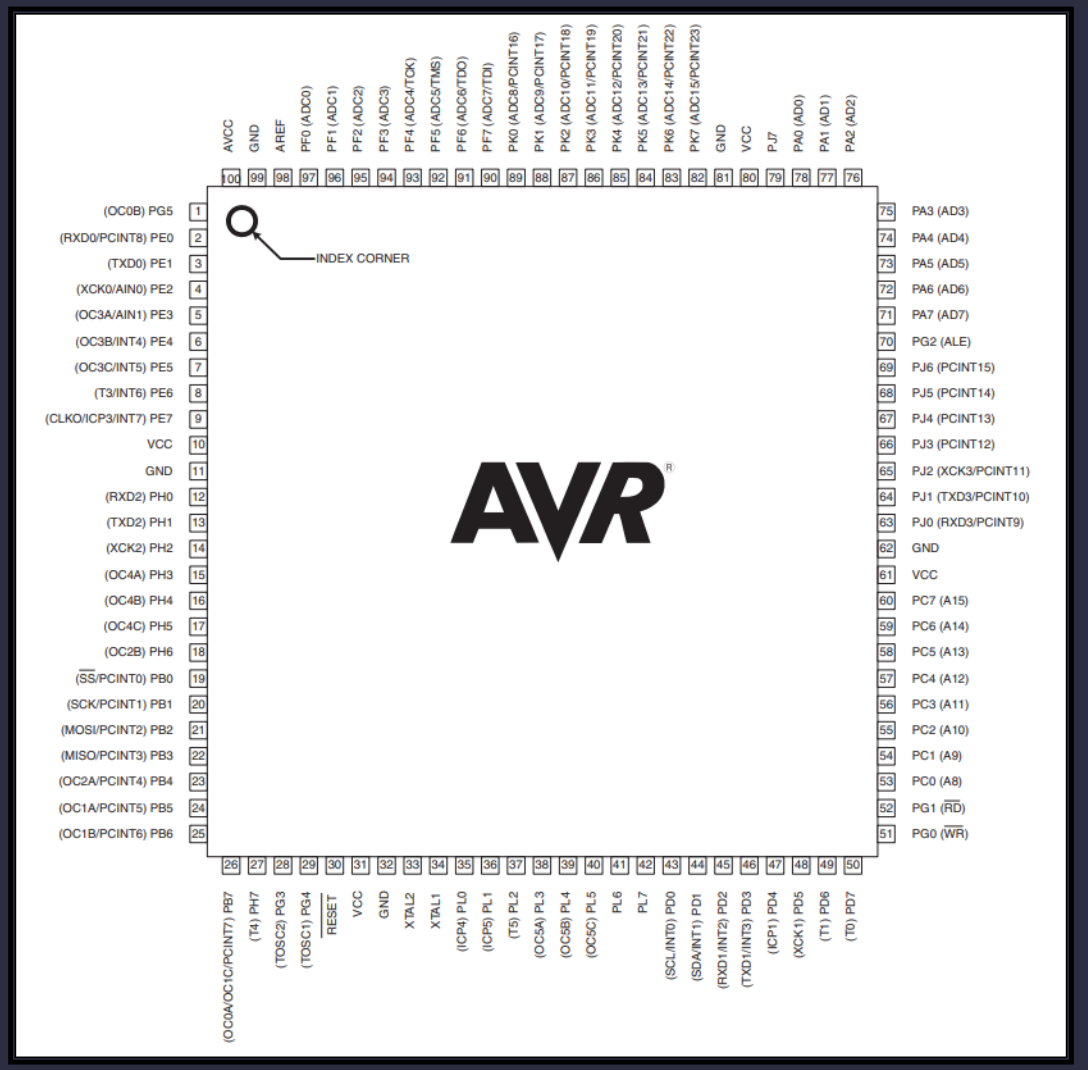
Table 1-1. CBGA-pinout ATmega640/1280/2560

	1	2	3	4	5	6	7	8	9	10
A	GND	AREF	PF0	PF2	PF5	PK0	PK3	PK6	GND	VCC
B	AVCC	PG5	PF1	PF3	PF6	PK1	PK4	PK7	PA0	PA2
C	PE2	PE0	PE1	PF4	PF7	PK2	PK5	PJ7	PA1	PA3
D	PE3	PE4	PE5	PE6	PH2	PA4	PA5	PA6	PA7	PG2
E	PE7	PH0	PH1	PH3	PH5	PJ6	PJ5	PJ4	PJ3	PJ2
F	VCC	PH4	PH6	PB0	PL4	PD1	PJ1	PJ0	PC7	GND
G	GND	PB1	PB2	PB5	PL2	PD0	PD5	PC5	PC6	VCC
H	PB3	PB4	RESET	PL1	PL3	PL7	PD4	PC4	PC3	PC2
J	PH7	PG3	PB6	PL0	XTAL2	PL6	PD3	PC1	PC0	PG1
K	PB7	PG4	VCC	GND	XTAL1	PL5	PD2	PD6	PD7	PG0

MCU & MPU Architectures, Interfaces

- Microcontroller Unit
  - Atmega2560 Architecture
  - Top Level View
    - TQFP Package Chip



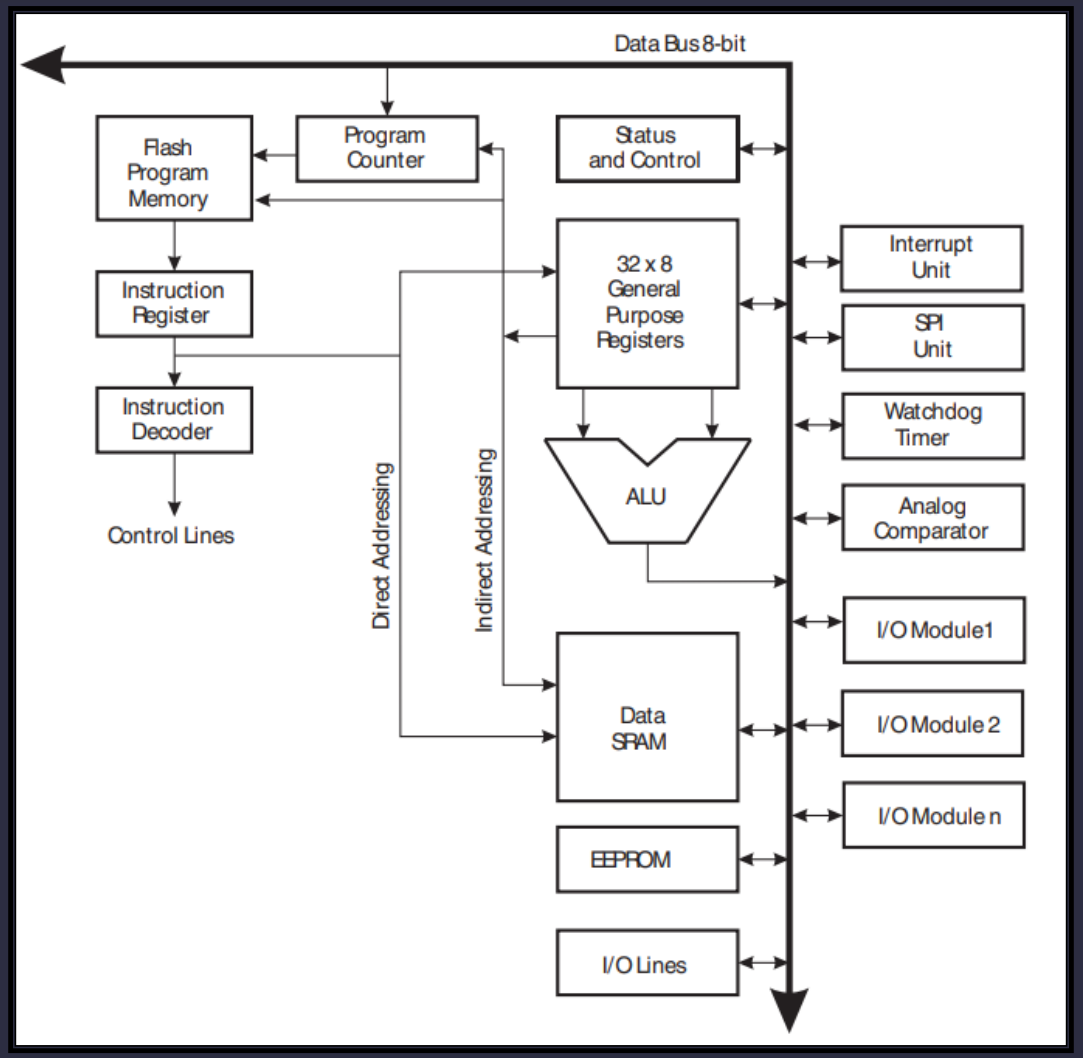


MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - Atmega2560 Architecture, MPU Core

  - Harvard Architecture – Separate program and data memory, single-level pipelining
  - Register File – 32 × 8-bit registers, single-cycle ALU operations
  - ALU Operations – Arithmetic, logic, single-register ops, Status Register updates
  - Program Memory – Flash, Boot/Application sections
  - Stack & Interrupts – Stack in SRAM, Interrupt Vector priority-based handling
  - I/O Memory – Direct & extended addressing, control registers in I/O space
  - 135 Instructions



MCU & MPU Architectures, Interfaces

- Microcontroller Unit
  - Atmega2560 Architecture, MPU Core
  - Arithmetic Instructions

ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z, C, N, V, H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z, C, N, V, H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z, C, N, V, S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z, C, N, V, H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z, C, N, V, H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z, C, N, V, H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z, C, N, V, H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z, C, N, V, S	2
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z, N, V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z, N, V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z, N, V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z, N, V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z, N, V	1
COM	Rd	One's Complement	Rd ← 0xFF – Rd	Z, C, N, V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z, C, N, V, H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z, N, V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • (0xFF - K)	Z, N, V	1
INC	Rd	Increment	Rd ← Rd + 1	Z, N, V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z, N, V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z, N, V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z, N, V	1
SER	Rd	Set Register	Rd ← 0xFF	None	1
MUL	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z, C	2
MULS	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z, C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z, C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z, C	2
FMULS	Rd, Rr	Fractional Multiply Signed	R1:R0 ← (Rd x Rr) << 1	Z, C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd x Rr) << 1	Z, C	2

MCU & MPU Architectures, Interfaces

- Microcontroller Unit
  - Atmega2560 Architecture, MPU Core
  - Branch Instructions

BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
EIJMP		Extended Indirect Jump to (Z)	PC ←(EIND:Z)	None	2
JMP	k	Direct Jump	PC ← k	None	3
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	4
ICALL		Indirect Call to (Z)	PC ← Z	None	4
EICALL		Extended Indirect Call to (Z)	PC ←(EIND:Z)	None	4
CALL	k	Direct Subroutine Call	PC ← k	None	5
RET		Subroutine Return	PC ← STACK	None	5
RETI		Interrupt Return	PC ← STACK	I	5
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd − Rr	Z, N, V, C, H	1
CPC	Rd,Rr	Compare with Carry	Rd − Rr − C	Z, N, V, C, H	1
CPI	Rd,K	Compare Register with Immediate	Rd − K	Z, N, V, C, H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2

MCU & MPU Architectures, Interfaces

- Microcontroller Unit
  - Atmega2560 Architecture, MPU Core
  - BIT Instructions

BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z, C, N, V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z, C, N, V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z, C, N, V	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z, C, N, V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z, C, N, V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1

MCU & MPU Architectures, Interfaces

- Microcontroller Unit
  - Atmega2560 Architecture, MPU Core
  - Data Transfer Instructions

DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
ELPM		Extended Load Program Memory	R0 ← (RAMPZ:Z)	None	3
ELPM	Rd, Z	Extended Load Program Memory	Rd ← (RAMPZ:Z)	None	3
ELPM	Rd, Z+	Extended Load Program Memory	Rd ← (RAMPZ:Z), RAMPZ:Z ←RAMPZ:Z+1	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1

MCU & MPU Architectures, Interfaces

- Microcontroller Unit
  - Atmega2560 Architecture, MPU Core
  - MCU Control Instructions

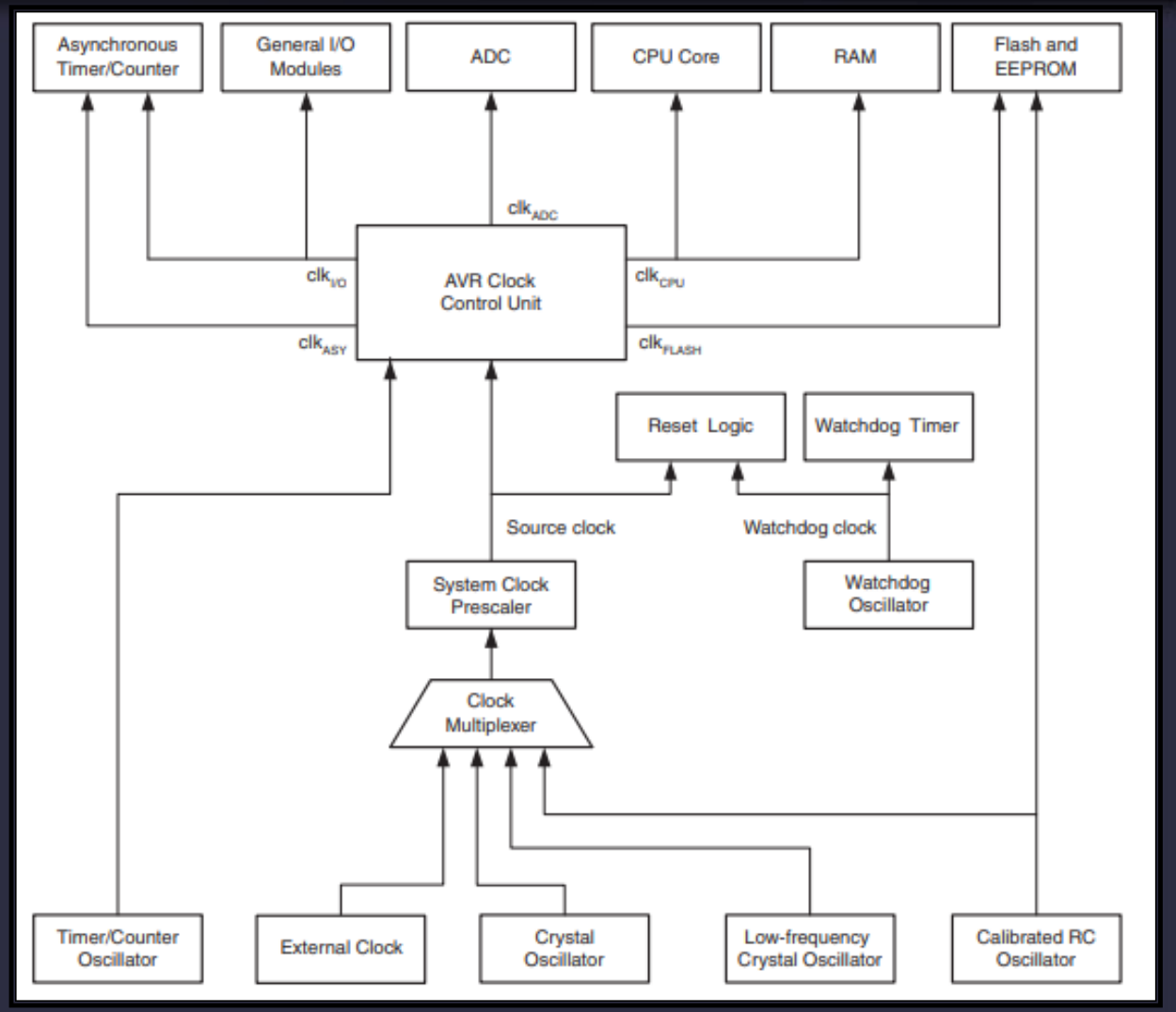
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - Atmega2560 Architecture

  - Clock Distribution – Multiple clocks, selective activation for power saving
  - CPU Clock (clkCPU) – Drives AVR core, registers, Stack Pointer
  - I/O Clock (clkI/O) – Used by I/O modules (Timers, SPI, USART, External Interrupts)
  - Flash Clock (clkFLASH) – Controls Flash interface, active with CPU clock
  - Asynchronous Timer Clock (clkASY) – Runs Timer/Counter independently, supports real-time functions in sleep mode
  - ADC Clock (clkADC) – Separate clock for ADC to reduce digital noise
  - Clock Sources – Selectable via Flash Fuse bits, multiple options available



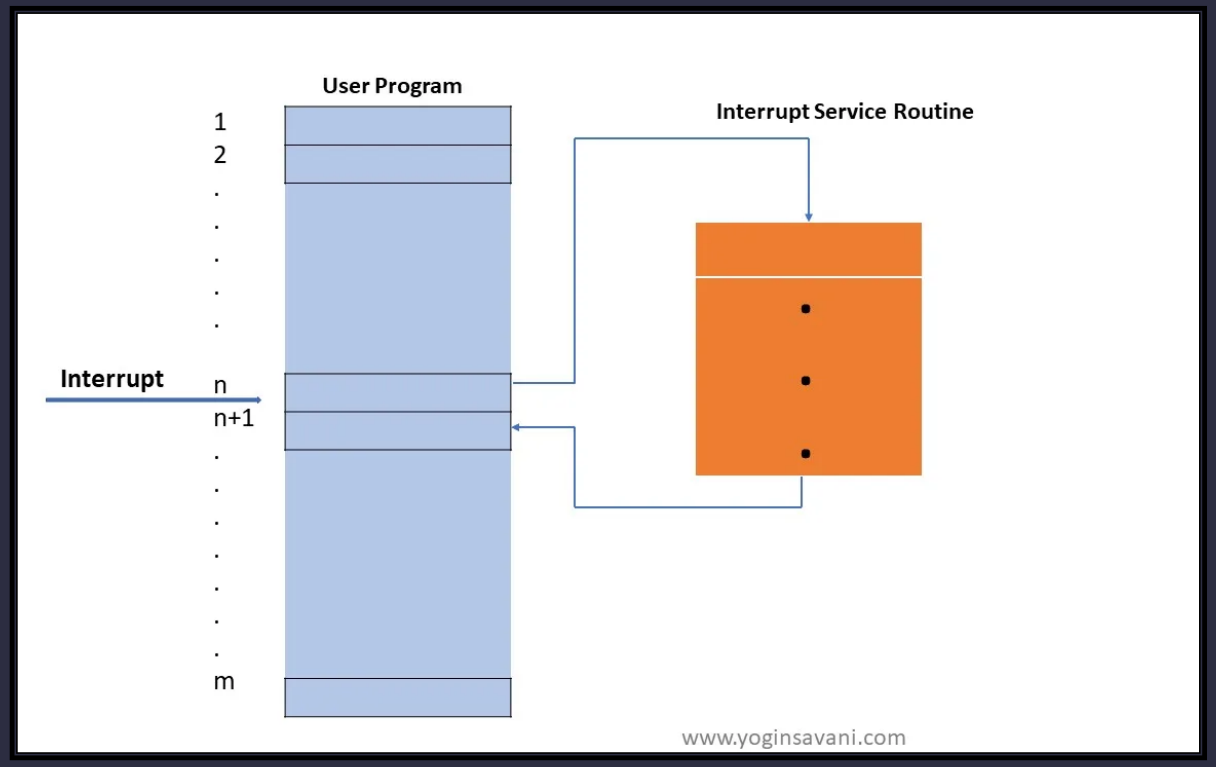
Clock Distribution

MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - Atmega2560 Architecture, Interrupt

  - Vector-Based Priority – Each interrupt has a unique vector; lower address = higher priority
  - Global Enable Bit (GIE) – Controlled via Status Register (SREG) to enable/disable all interrupts
  - Automatic Context Saving – Program Counter (PC) stored in Stack on interrupt trigger
  - Nested Interrupts – Possible if interrupts are re-enabled inside an ISR



MCU & MPU Architectures, Interfaces

- Microcontroller Unit
  - Atmega2560 Architecture, Interrupt
  - Vector 1

Vector No.	Program Address(2)	Source	Interrupt Definition
1	$0000(1)	RESET	External Pin, Power-on Reset, Brown-out Reset, Watchdog Reset, and JTAG AVR Reset
2	$0002	INT0	External Interrupt Request 0
3	$0004	INT1	External Interrupt Request 1
4	$0006	INT2	External Interrupt Request 2
5	$0008	INT3	External Interrupt Request 3
6	$000A	INT4	External Interrupt Request 4
7	$000C	INT5	External Interrupt Request 5
8	$000E	INT6	External Interrupt Request 6
9	$0010	INT7	External Interrupt Request 7
10	$0012	PCINT0	Pin Change Interrupt Request 0
11	$0014	PCINT1	Pin Change Interrupt Request 1
12	$0016(3)	PCINT2	Pin Change Interrupt Request 2
13	$0018	WDT	Watchdog Time-out Interrupt
14	$001A	TIMER2 COMPA	Timer/Counter2 Compare Match A
15	$001C	TIMER2 COMPB	Timer/Counter2 Compare Match B
16	$001E	TIMER2 OVF	Timer/Counter2 Overflow
17	$0020	TIMER1 CAPT	Timer/Counter1 Capture Event
18	$0022	TIMER1 COMPA	Timer/Counter1 Compare Match A
19	$0024	TIMER1 COMPB	Timer/Counter1 Compare Match B
20	$0026	TIMER1 COMPC	Timer/Counter1 Compare Match C
21	$0028	TIMER1 OVF	Timer/Counter1 Overflow
22	$002A	TIMER0 COMPA	Timer/Counter0 Compare Match A
23	$002C	TIMER0 COMPB	Timer/Counter0 Compare match B
24	$002E	TIMER0 OVF	Timer/Counter0 Overflow
25	$0030	SPI, STC	SPI Serial Transfer Complete
26	$0032	USART0 RX	USART0 Rx Complete
27	$0034	USART0 UDRE	USART0 Data Register Empty
28	$0036	USART0 TX	USART0 Tx Complete
29	$0038	ANALOG COMP	Analog Comparator
30	$003A	ADC	ADC Conversion Complete

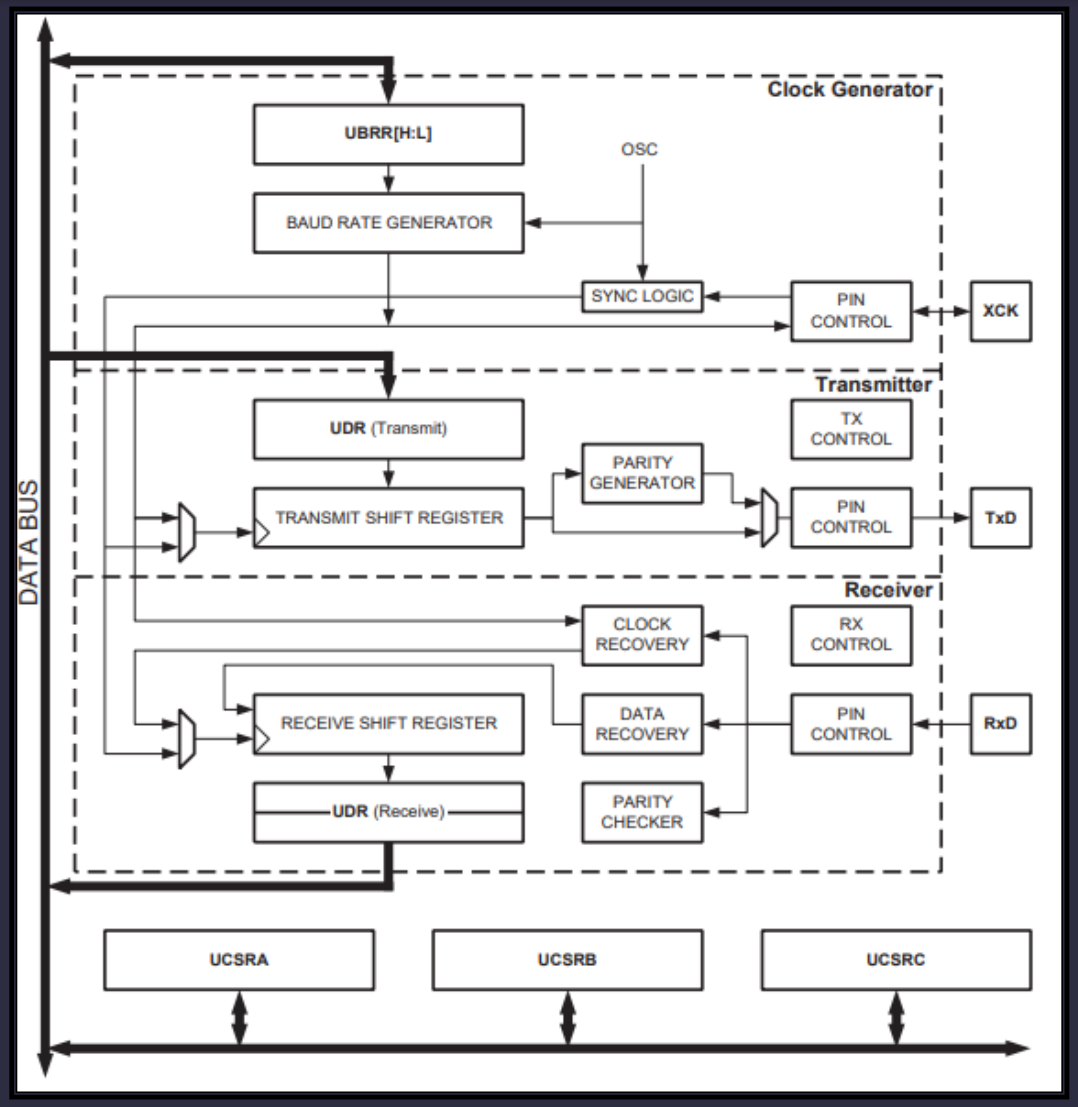
MCU & MPU Architectures, Interfaces

- Microcontroller Unit
  - Atmega2560 Architecture, Interrupt
  - Vector 2

Vector No.	Program Address(2)	Source	Interrupt Definition
31	$003C	EE READY	EEPROM Ready
32	$003E	TIMER3 CAPT	Timer/Counter3 Capture Event
33	$0040	TIMER3 COMPA	Timer/Counter3 Compare Match A
34	$0042	TIMER3 COMPB	Timer/Counter3 Compare Match B
35	$0044	TIMER3 COMPC	Timer/Counter3 Compare Match C
36	$0046	TIMER3 OVF	Timer/Counter3 Overflow
37	$0048	USART1 RX	USART1 Rx Complete
38	$004A	USART1 UDRE	USART1 Data Register Empty
39	$004C	USART1 TX	USART1 Tx Complete
40	$004E	TWI	2-wire Serial Interface
41	$0050	SPM READY	Store Program Memory Ready
42	$0052(3)	TIMER4 CAPT	Timer/Counter4 Capture Event
43	$0054	TIMER4 COMPA	Timer/Counter4 Compare Match A
44	$0056	TIMER4 COMPB	Timer/Counter4 Compare Match B
45	$0058	TIMER4 COMPC	Timer/Counter4 Compare Match C
46	$005A	TIMER4 OVF	Timer/Counter4 Overflow
47	$005C(3)	TIMER5 CAPT	Timer/Counter5 Capture Event
48	$005E	TIMER5 COMPA	Timer/Counter5 Compare Match A
49	$0060	TIMER5 COMPB	Timer/Counter5 Compare Match B
50	$0062	TIMER5 COMPC	Timer/Counter5 Compare Match C
51	$0064	TIMER5 OVF	Timer/Counter5 Overflow
52	$0066(3)	USART2 RX	USART2 Rx Complete
53	$0068(3)	USART2 UDRE	USART2 Data Register Empty
54	$006A(3)	USART2 TX	USART2 Tx Complete
55	$006C(3)	USART3 RX	USART3 Rx Complete
56	$006E(3)	USART3 UDRE	USART3 Data Register Empty
57	$0070(3)	USART3 TX	USART3 Tx Complete

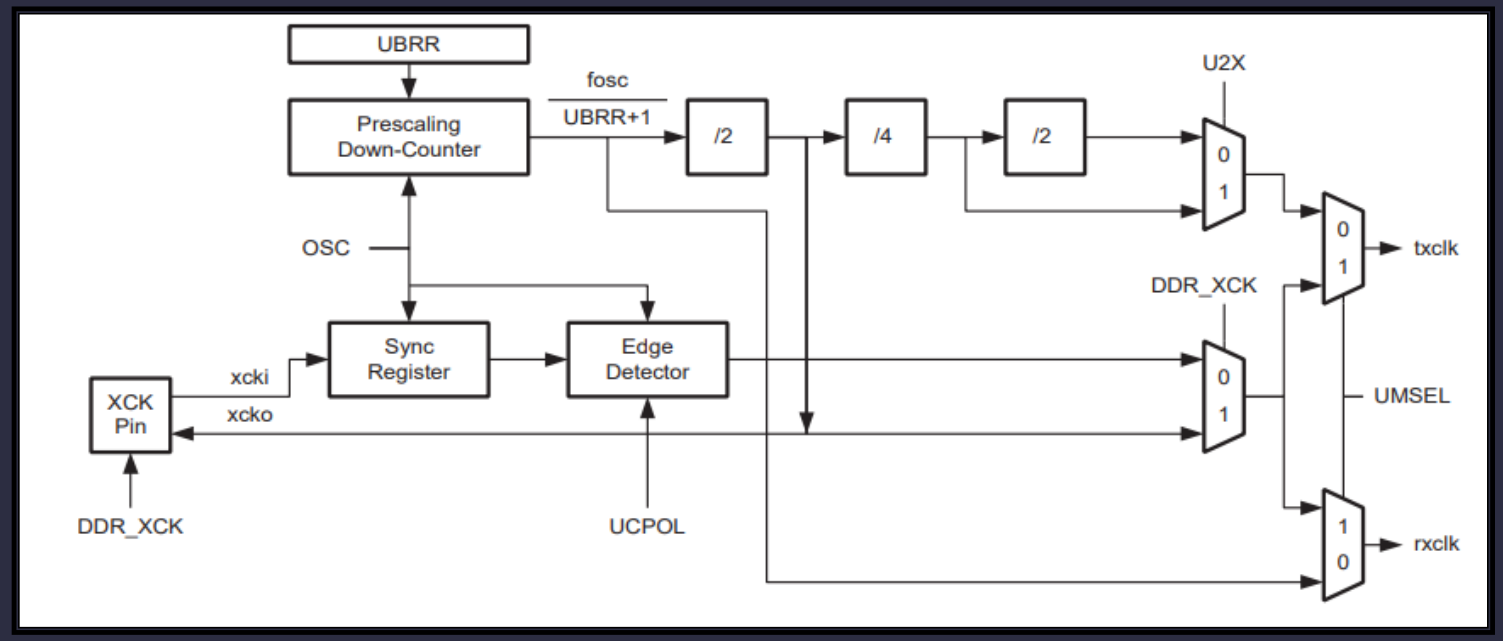
MCU & MPU Architectures, Interfaces

- Interfaces
  - Atmega2560 Architecture, UART
  - General Overview



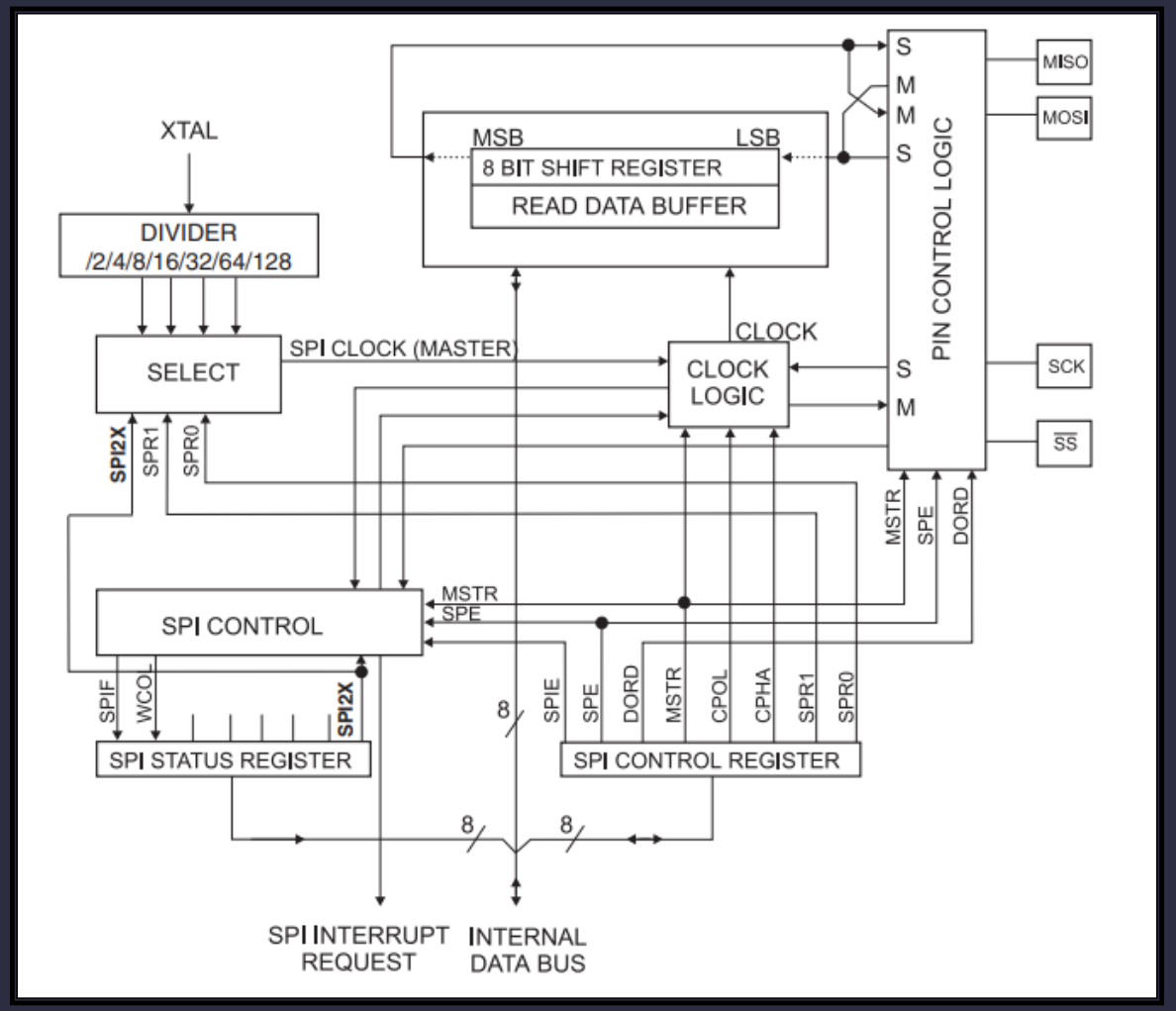
MCU & MPU Architectures, Interfaces

- Interfaces
  - Atmega2560 Architecture, UART
  - Baud Rate Set



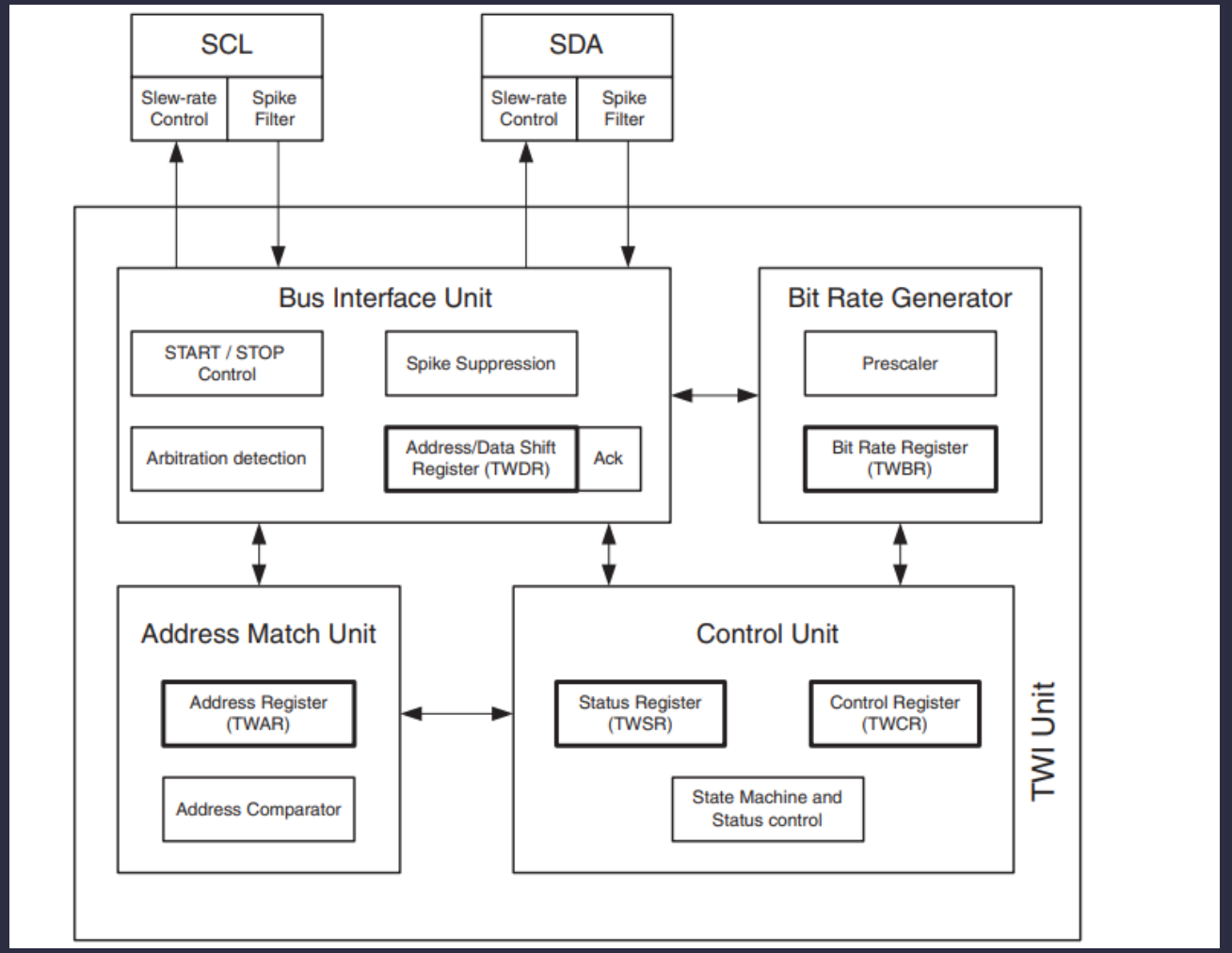
MCU & MPU Architectures, Interfaces

- Interfaces
  - Atmega2560 Architecture, SPI
  - SPI Overview



MCU & MPU Architectures, Interfaces

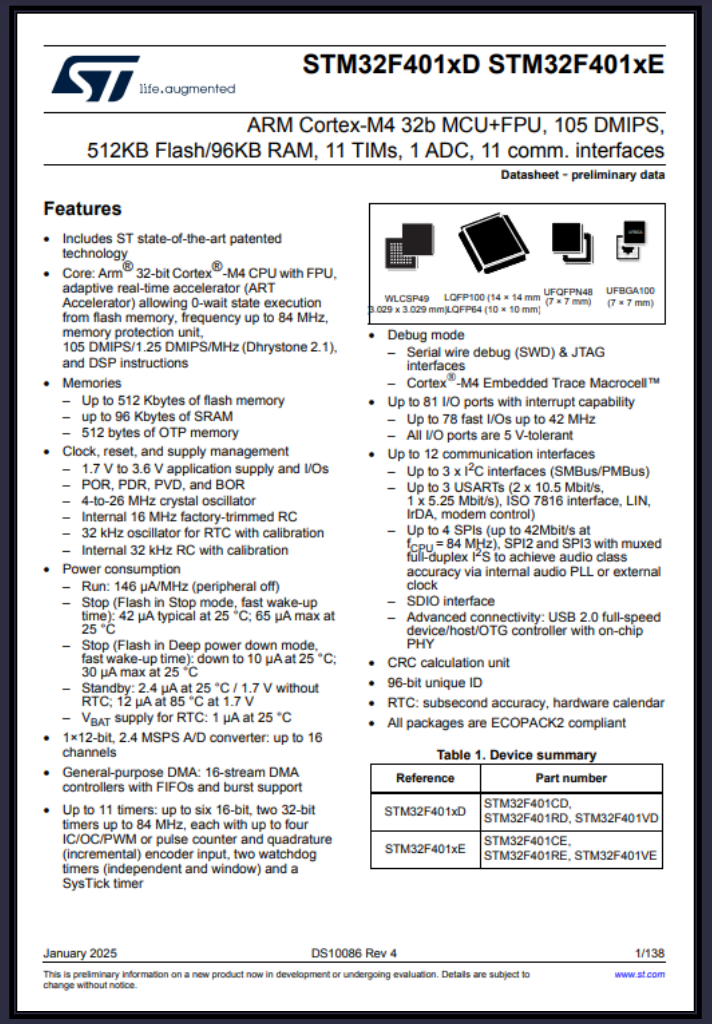
- Interfaces
  - Atmega2560 Architecture, I2C – Two Wire
  - Two Wire Interface Overview



MCU & MPU Architectures, Interfaces

- Microcontroller Unit

  - Use Cases
    - STM32F401RE, ST Microelectronic
    - Datasheet: https://www.st.com/resource/en/datasheet/stm32f401re.pdf



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STM32F401xD STM32F401xE

ARM Cortex-M4 32b MCU+FPU, 105 DMIPS, 512KB Flash/96KB RAM, 11 TIMs, 1 ADC, 11 comm. interfaces

Datasheet - preliminary data

Features

- Includes ST state-of-the-art patented technology
- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, adaptive real-time accelerator (ART Accelerator) allowing 0-wait state execution from flash memory, frequency up to 84 MHz, memory protection unit, 105 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - Up to 512 Kbytes of flash memory
  - up to 96 Kbytes of SRAM
  - 512 bytes of OTP memory
- Clock, reset, and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD, and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Power consumption
  - Run: 146 µA/MHz (peripheral off)
  - Stop (Flash in Stop mode, fast wake-up time): 42 µA typical at 25 °C; 65 µA max at 25 °C
  - Stop (Flash in Deep power down mode, fast wake-up time): down to 10 µA at 25 °C; 30 µA max at 25 °C
  - Standby: 2.4 µA at 25 °C / 1.7 V without RTC; 12 µA at 85 °C at 1.7 V
  - V_{BAT} supply for RTC: 1 µA at 25 °C
- 1×12-bit, 2.4 MSPS A/D converter: up to 16 channels
- General-purpose DMA: 16-stream DMA controllers with FIFOs and burst support
- Up to 11 timers: up to six 16-bit, two 32-bit timers up to 84 MHz, each with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input, two watchdog timers (independent and window) and a SysTick timer

WLCSP49 (3.029 x 3.029 mm) LQFP100 (14 × 14 mm) LQFP64 (10 × 10 mm) UFQFPN48 (7 × 7 mm) UFBGA100 (7 × 7 mm)

- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex®-M4 Embedded Trace Macrocell™
- Up to 81 I/O ports with interrupt capability
  - Up to 78 fast I/Os up to 42 MHz
  - All I/O ports are 5 V-tolerant
- Up to 12 communication interfaces
  - Up to 3 x I^2C interfaces (SMBus/PMBus)
  - Up to 3 USARTs (2 x 10.5 Mbit/s, 1 x 5.25 Mbit/s), ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 4 SPIs (up to 42Mbit/s at f_{CPU} = 84 MHz), SPI2 and SPI3 with muxed full-duplex I^2S to achieve audio class accuracy via internal audio PLL or external clock
  - SDIO interface
  - Advanced connectivity: USB 2.0 full-speed device/host/OTG controller with on-chip PHY
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar
- All packages are ECOPACK2 compliant

Table 1. Device summary

Reference	Part number
STM32F401xD	STM32F401CD, STM32F401RD, STM32F401VD
STM32F401xE	STM32F401CE, STM32F401RE, STM32F401VE

January 2025 DS10086 Rev 4 1/138

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice. www.st.com

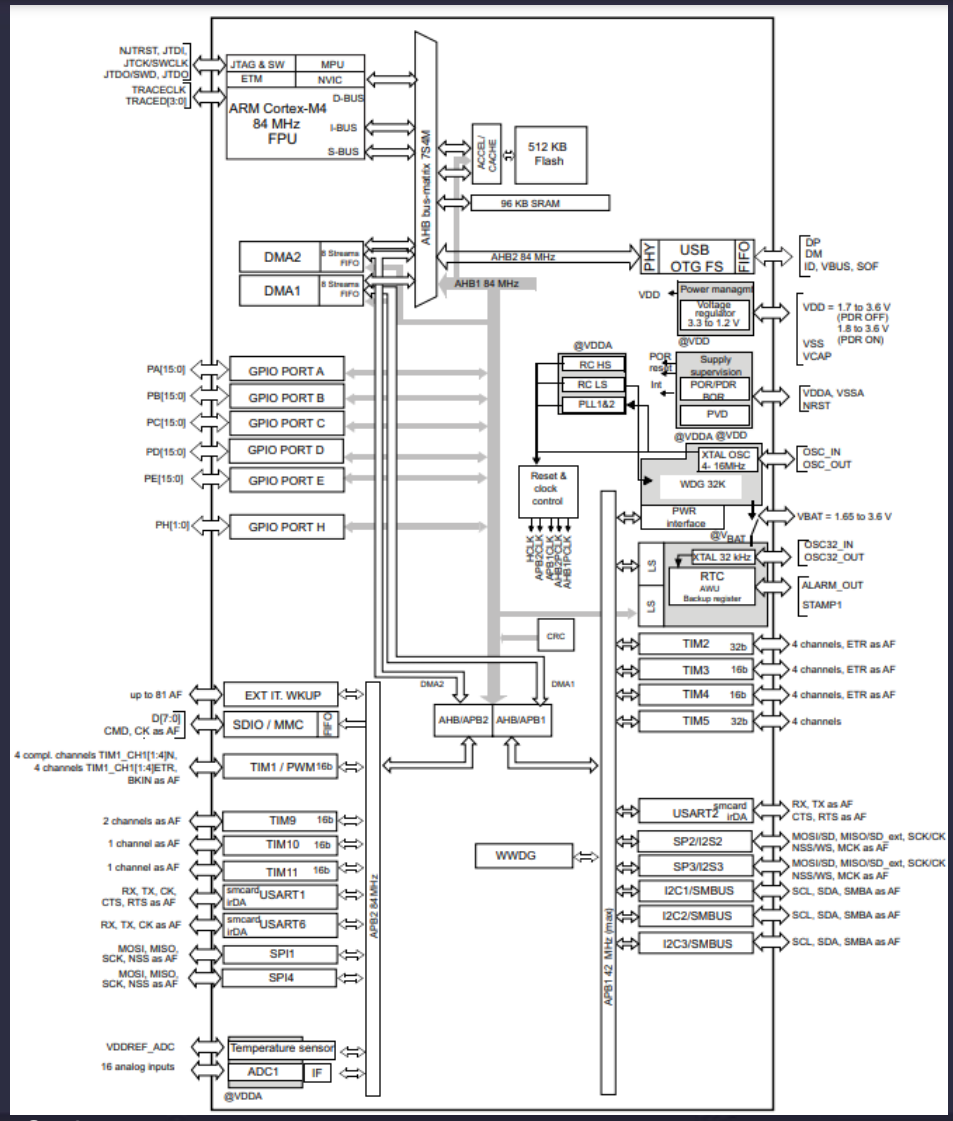
138 Pages

MCU & MPU Architectures, Interfaces

- Microcontroller Unit

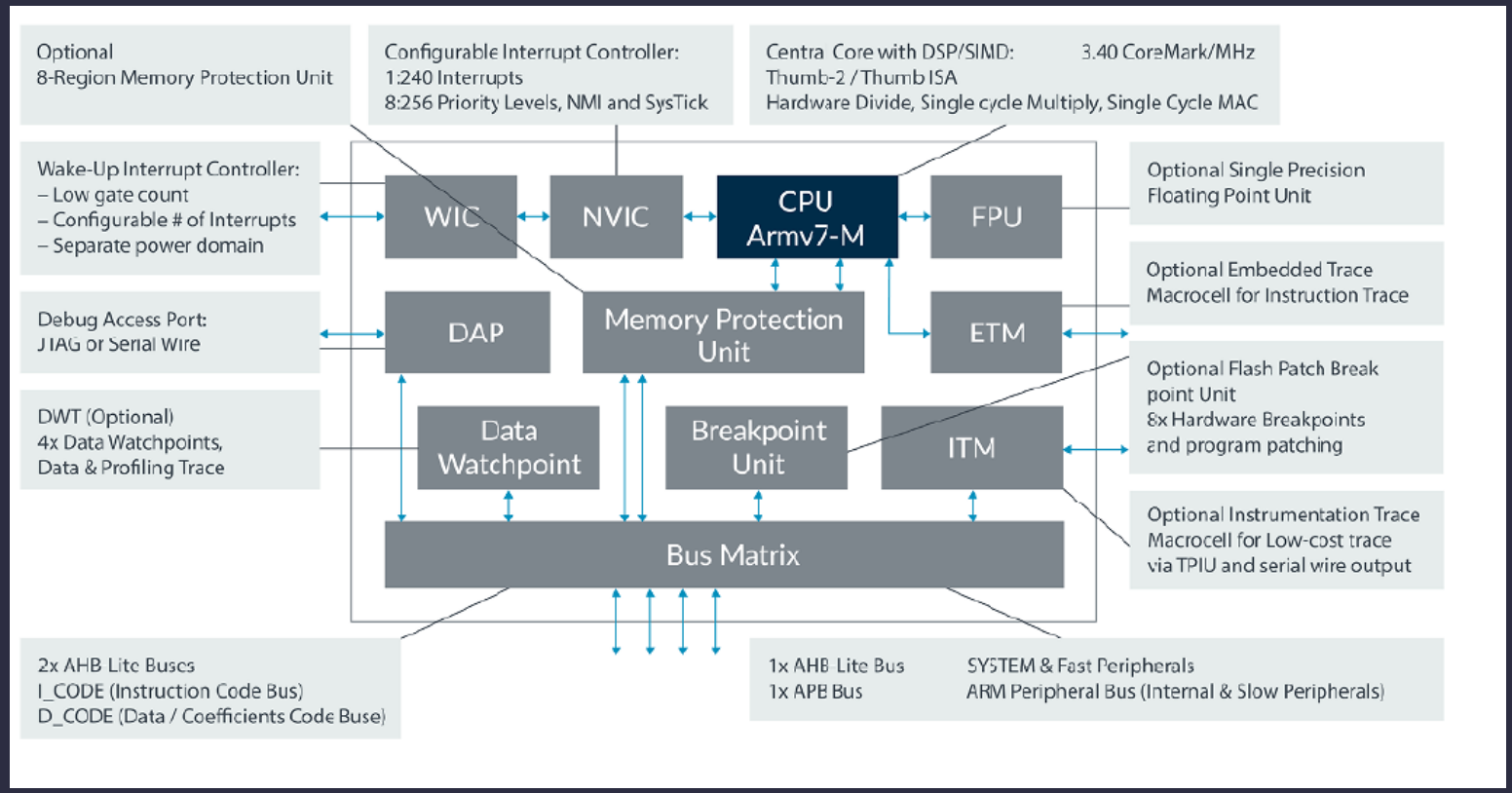
- STM32F401RE Architecture

- Core: Arm® 32-bit Cortex®-M4 CPU with FPU,
- adaptive real-time accelerator (ART Accelerator) allowing 0-wait state execution from flash memory, frequency up to 84 MHz, memory protection unit,
- 105 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1),
- and DSP instructions
- Memories
  - Up to 512 Kbytes of flash memory
  - up to 96 Kbytes of SRAM
  - 512 bytes of OTP memory
- Clock, reset, and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - 4-to-26 MHz crystal oscillator



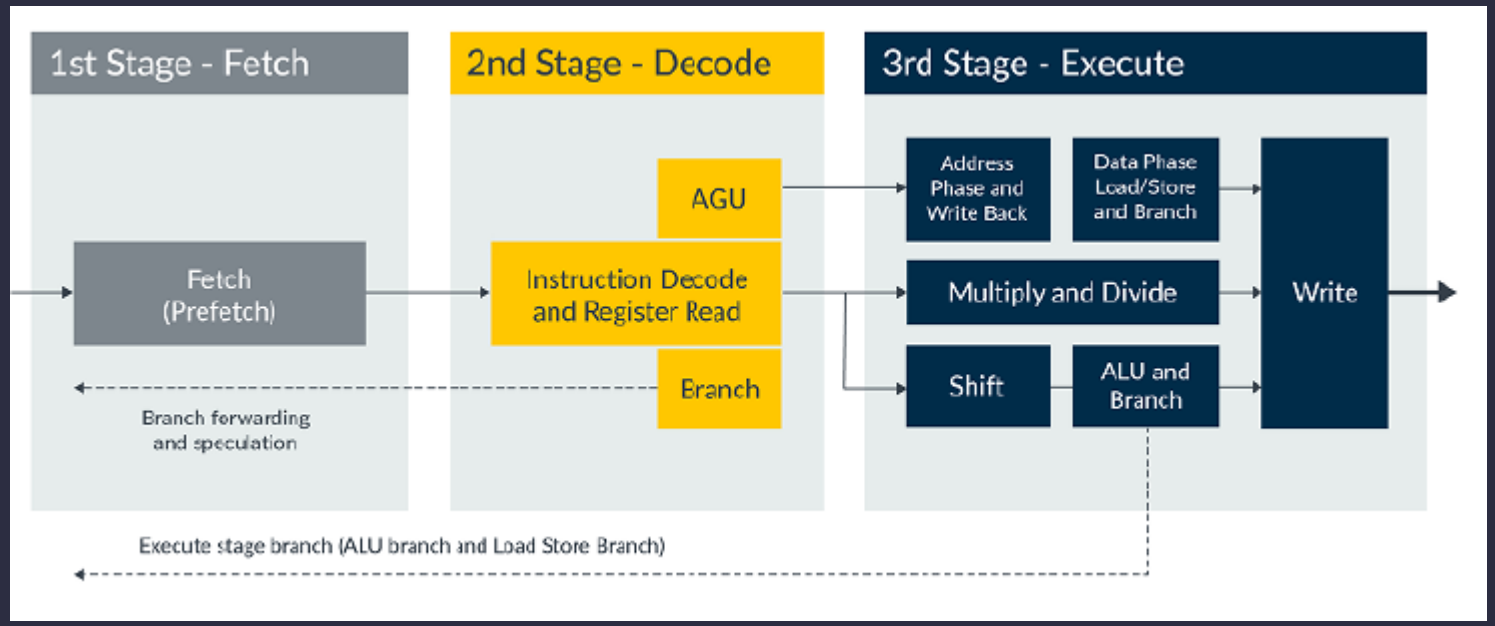
MCU & MPU Architectures, Interfaces

- Microcontroller Unit
- STM32F401RE Architecture
- Arm® 32-bit Cortex®-M4 CPU



MCU & MPU Architectures, Interfaces

- Microcontroller Unit
- STM32F401RE Architecture
- Arm® 32-bit Cortex®-M4 CPU



MCU & MPU Architectures, Interfaces

- Microcontroller Unit
- STM32F401RE Architecture
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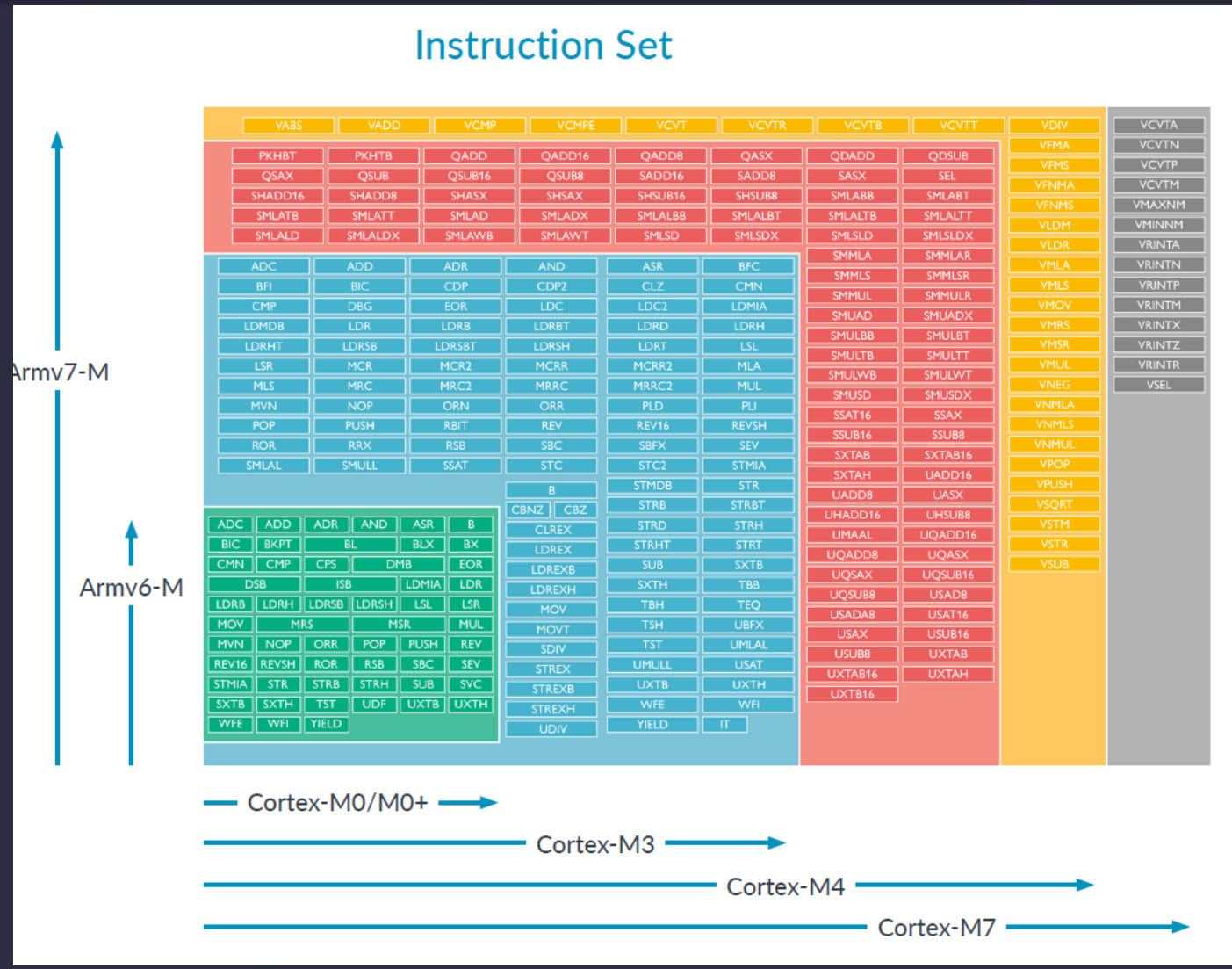


MCU & MPU Architectures, Interfaces

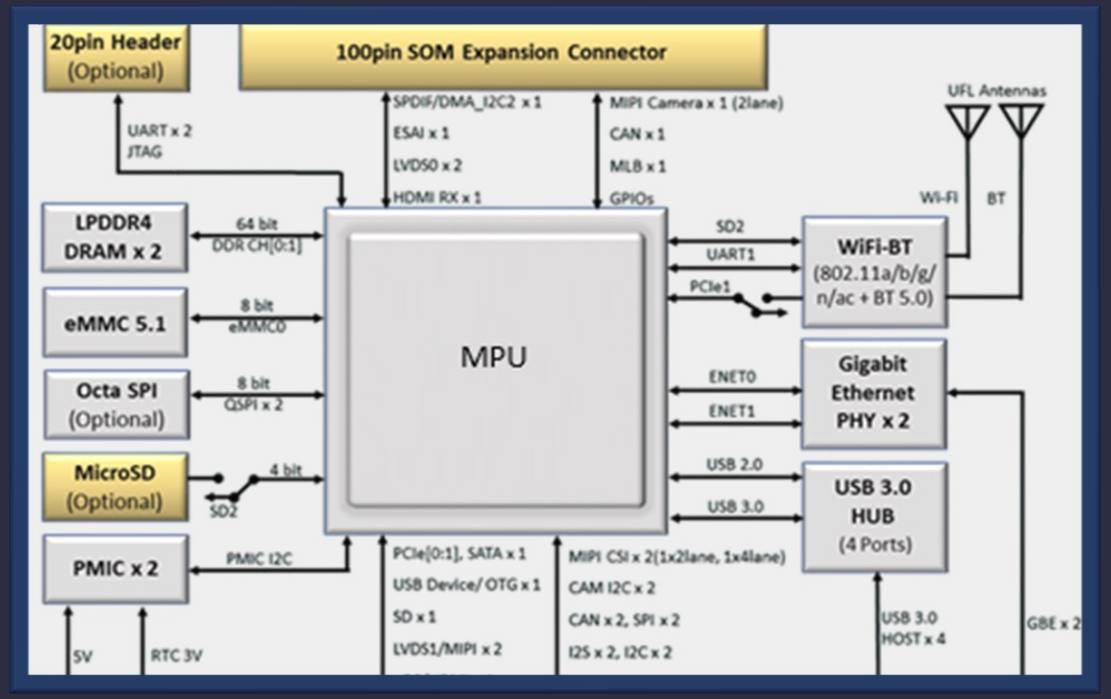
- Microcontroller Unit
- Atmega2560 vs STM32F401RE

Feature	STM32F401RE	ATmega2560
Architecture	ARM Cortex-M4	AVR 8-bit
Clock Speed	84 MHz	16 MHz
Flash Memory	512 KB	256 KB
RAM	96 KB	8 KB
Operating Voltage	3.3V	5V
GPIOs	50	86
Timers	10 (including advanced timers)	6
ADC	12-bit, 16 channels	10-bit, 16 channels
DAC	12-bit, 2 channels	No DAC
PWM	Yes, advanced	Yes, basic
UART/I2C/SPI	3x UART, 3x I2C, 3x SPI	4x UART, 2x I2C, 1x SPI
USB Support	Yes, Full-Speed	Yes, Full-Speed
External Interrupts	Yes, advanced	Yes, basic
Power Consumption	Lower	Higher
Development Tools	Keil, STM32CubeIDE, IAR	Arduino, AVR Studio, Atmel Studio

Feature	STM32F401RE	ATmega2560
Processing Power	✅ Much faster (84 MHz, ARM Cortex-M4 with FPU)	❌ Slower (16 MHz, 8-bit AVR)
Memory	✅ More RAM (96 KB) & Flash (512 KB)	❌ Limited RAM (8 KB) & Flash (256 KB)
Power Efficiency	✅ Lower power (3.3V)	❌ Higher power (5V)
ADC & DAC	✅ 12-bit ADC + DAC	❌ 10-bit ADC, no DAC
GPIO Count	❌ Fewer GPIOs	✅ More GPIOs
Development Support	❌ More complex (requires STM32Cube, Keil, etc.)	✅ Easier with Arduino IDE
Interrupt Handling	✅ More advanced	❌ Basic interrupts

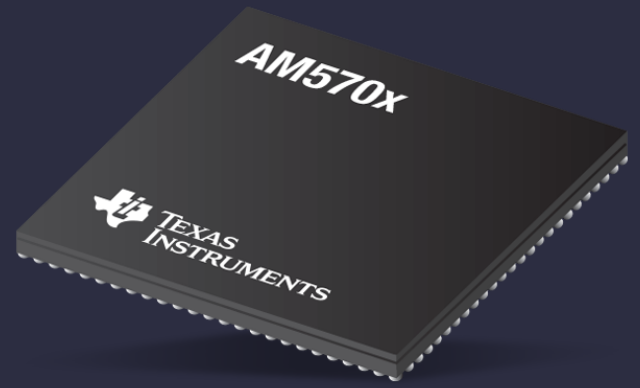
MCU & MPU Architectures, Interfaces

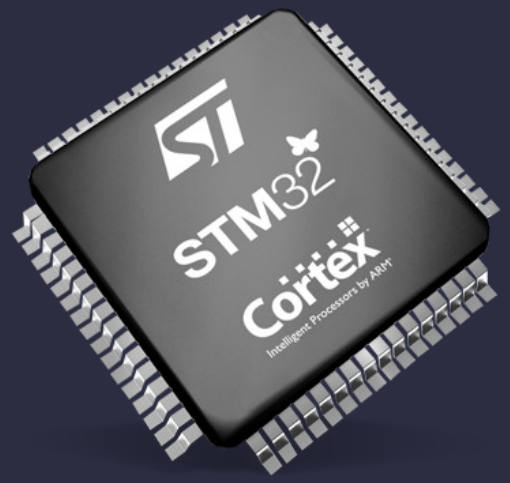
- Microprocessor Unit
  - MPU (Microprocessor Unit)
    - Works with external RAM and storage, often used in embedded Linux systems.
    - More powerful than an MCU but not as strong as a CPU.
    - Handles higher-performance tasks requiring an OS.
    - Average Frequency: 500 MHz - 2.5 GHz
    - Average FLOPS: 1 GFLOPS - 10 GFLOPS

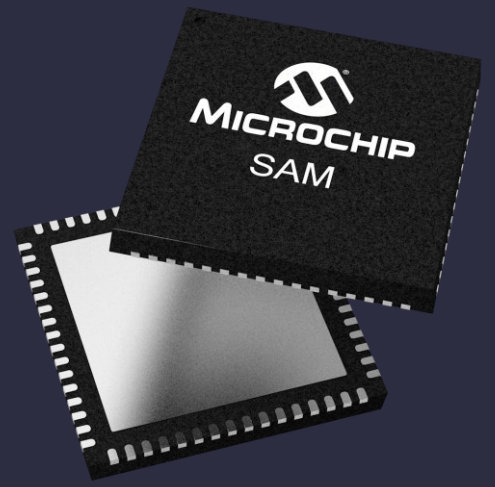


MCU & MPU Architectures, Interfaces

- Microprocessor Unit
  - MPU (Microprocessor Unit)
  - Vendors
    - NXP Semiconductors (i.MX)
    - Texas Instruments (Sitara)
    - ST Microelectronics (STM32)
    - Microchip Technology (SAM)

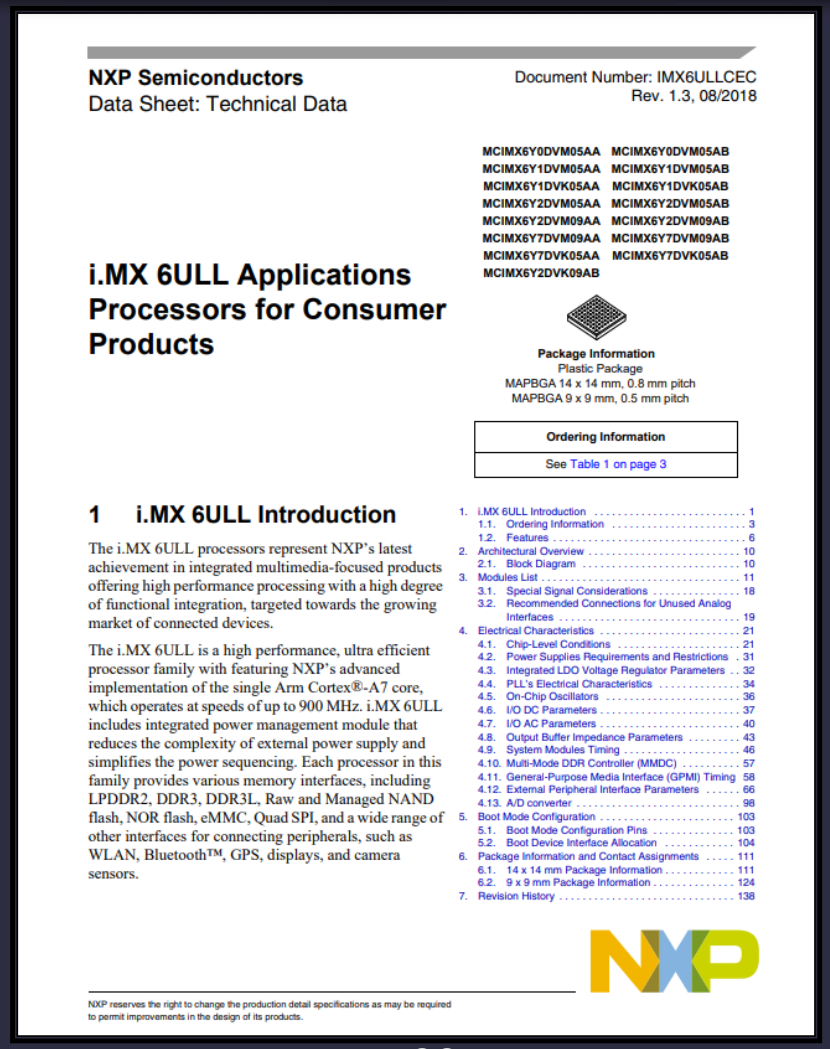






MCU & MPU Architectures, Interfaces

- Microprocessor Unit
  - Use Case
    - i.MX 6 MPU
    - Datasheet: https://www.nxp.com/docs/en/data-sheet/IMX6ULLCEC.pdf



NXP Semiconductors
Data Sheet: Technical Data

Document Number: IMX6ULLCEC
Rev. 1.3, 08/2018

MCIMX6Y0DVM05AA MCIMX6Y0DVM05AB
MCIMX6Y1DVM05AA MCIMX6Y1DVM05AB
MCIMX6Y1DVK05AA MCIMX6Y1DVK05AB
MCIMX6Y2DVM05AA MCIMX6Y2DVM05AB
MCIMX6Y2DVM09AA MCIMX6Y2DVM09AB
MCIMX6Y7DVM09AA MCIMX6Y7DVM09AB
MCIMX6Y7DVK05AA MCIMX6Y7DVK05AB
MCIMX6Y2DVK09AB

i.MX 6ULL Applications Processors for Consumer Products

Package Information
Plastic Package
MAPBGA 14 x 14 mm, 0.8 mm pitch
MAPBGA 9 x 9 mm, 0.5 mm pitch

Ordering Information
See Table 1 on page 3

1 i.MX 6ULL Introduction

The i.MX 6ULL processors represent NXP's latest achievement in integrated multimedia-focused products offering high performance processing with a high degree of functional integration, targeted towards the growing market of connected devices.

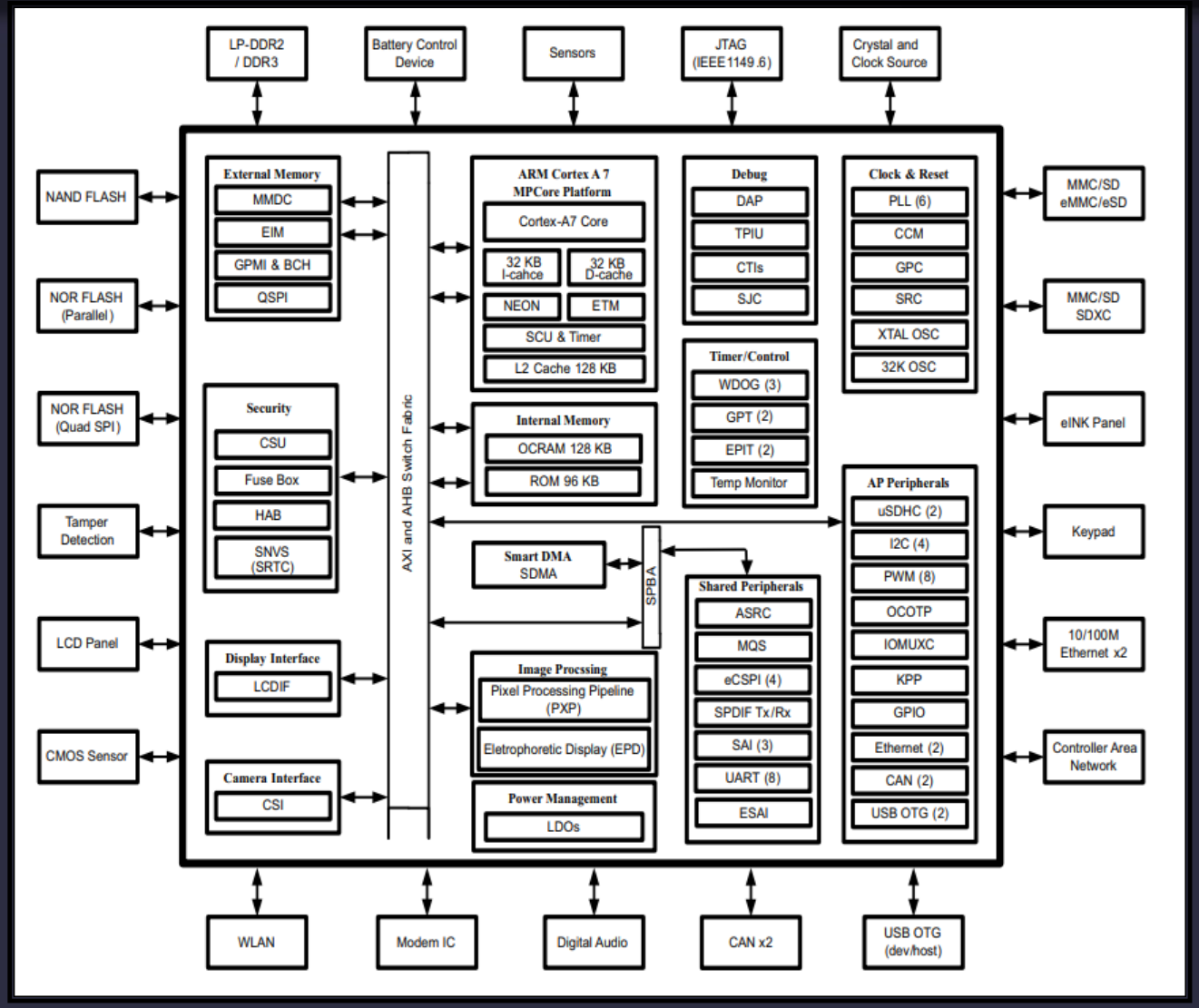
The i.MX 6ULL is a high performance, ultra efficient processor family with featuring NXP's advanced implementation of the single Arm Cortex®-A7 core, which operates at speeds of up to 900 MHz. i.MX 6ULL includes integrated power management module that reduces the complexity of external power supply and simplifies the power sequencing. Each processor in this family provides various memory interfaces, including LPDDR2, DDR3, DDR3L, Raw and Managed NAND flash, NOR flash, eMMC, Quad SPI, and a wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors.

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

139 Pages

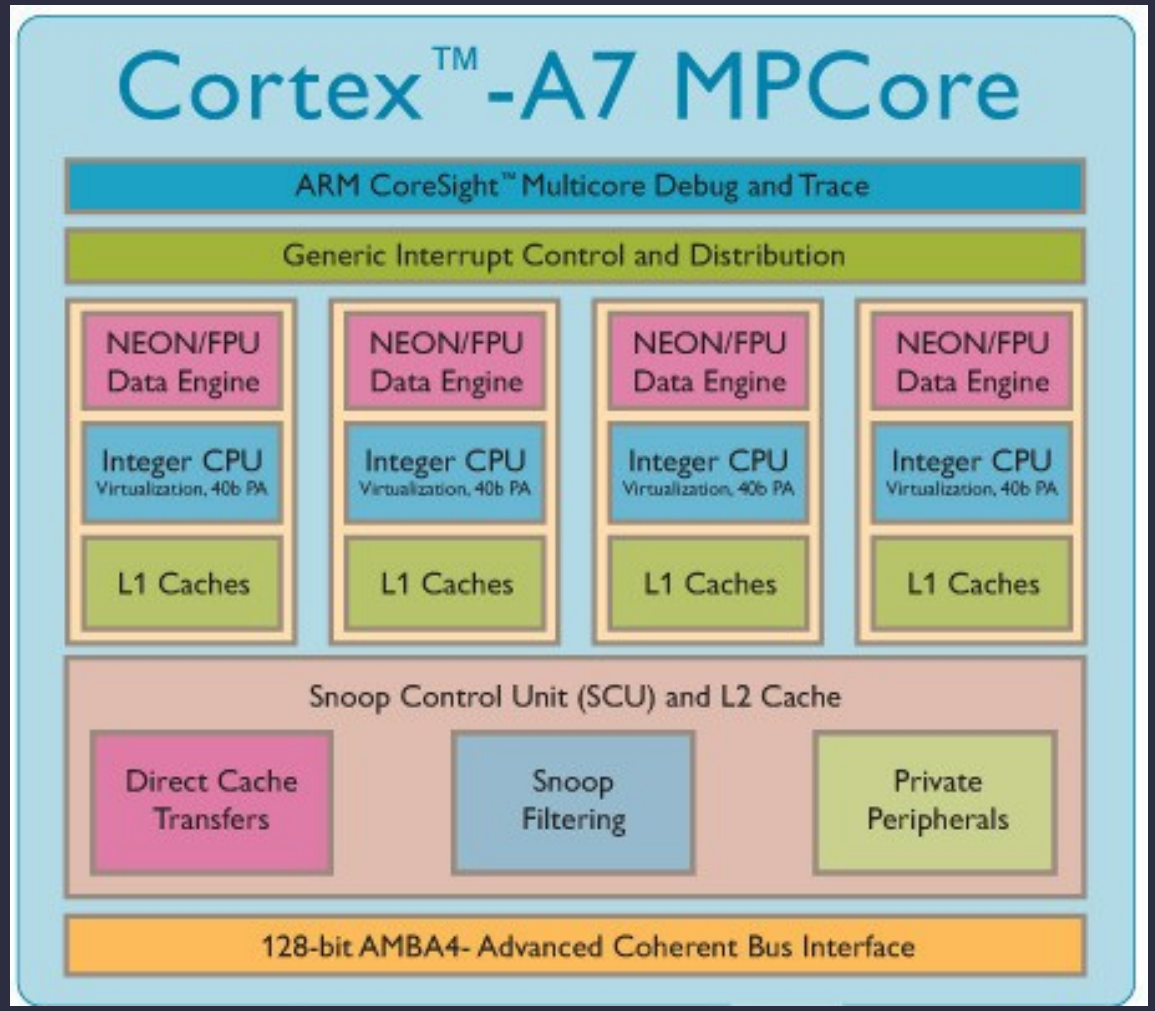
MCU & MPU Architectures, Interfaces

- Microprocessor Unit
  - i.MX 6 Overview



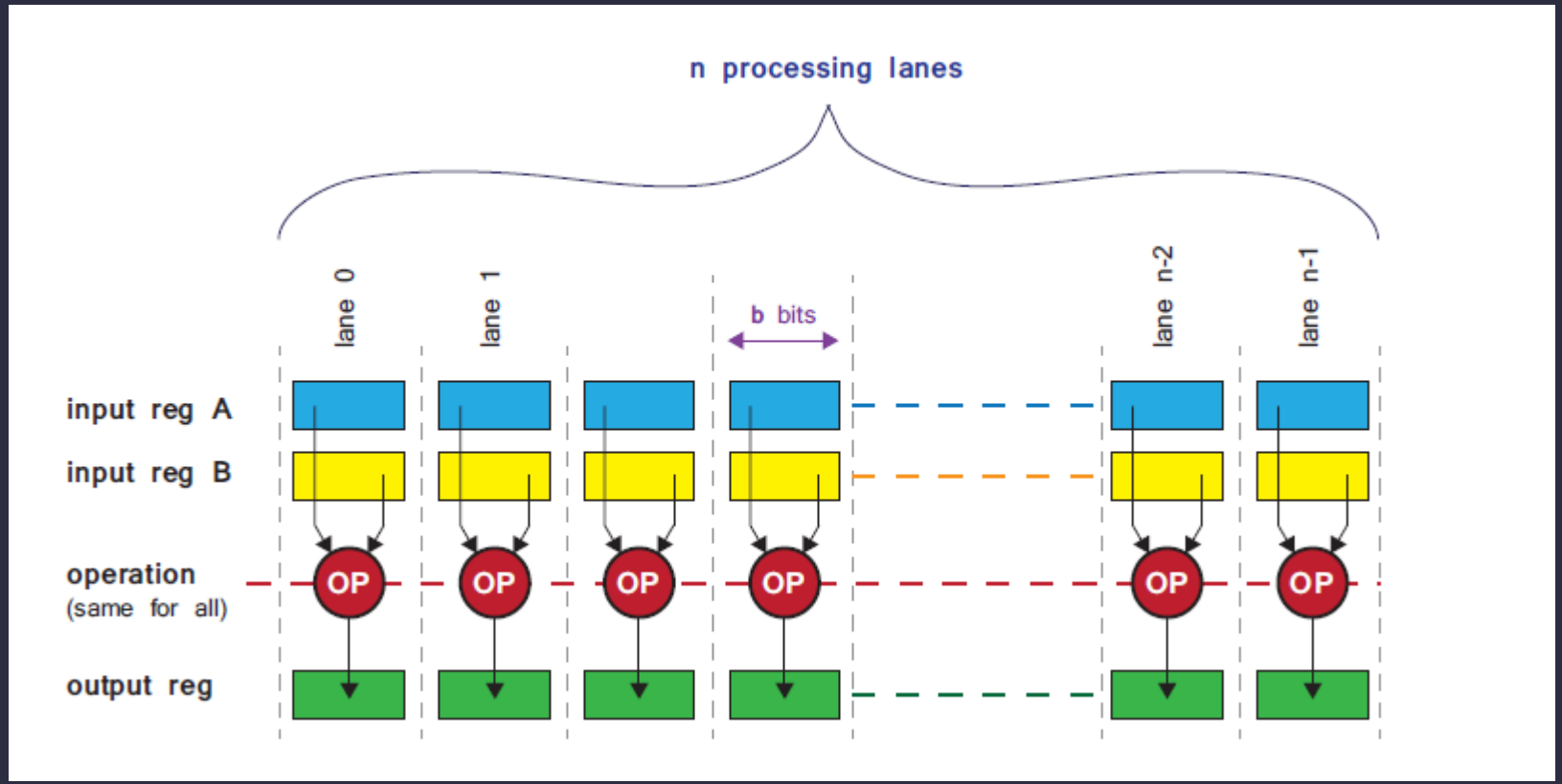
MCU & MPU Architectures, Interfaces

- Microprocessor Unit
  - i.MX 6 Overview
  - ARM Cortex A7 CPU Architecture



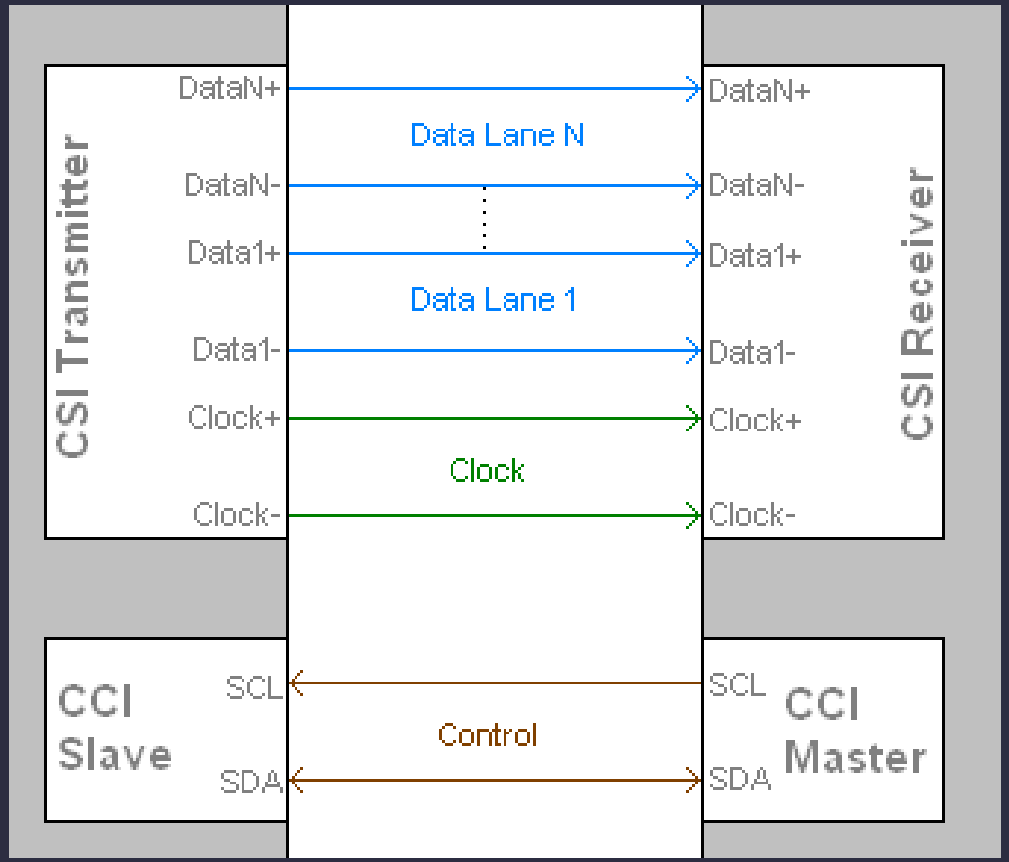
MCU & MPU Architectures, Interfaces

- Microprocessor Unit
  - i.MX 6 Overview
  - NEON Engine
  - Single Instruction Multiple Data (SIMD) processing in the NEON MPE



MCU & MPU Architectures, Interfaces

- Microprocessor Unit
  - i.MX 6 Overview
  - MPU Blocks
  - CSI Camera Receiver



MCU & MPU Architectures, Interfaces

- Microprocessor Unit

  - i.MX 6 Overview
  - MPU Blocks

  - eCSPI (Enhanced Configurable SPI)

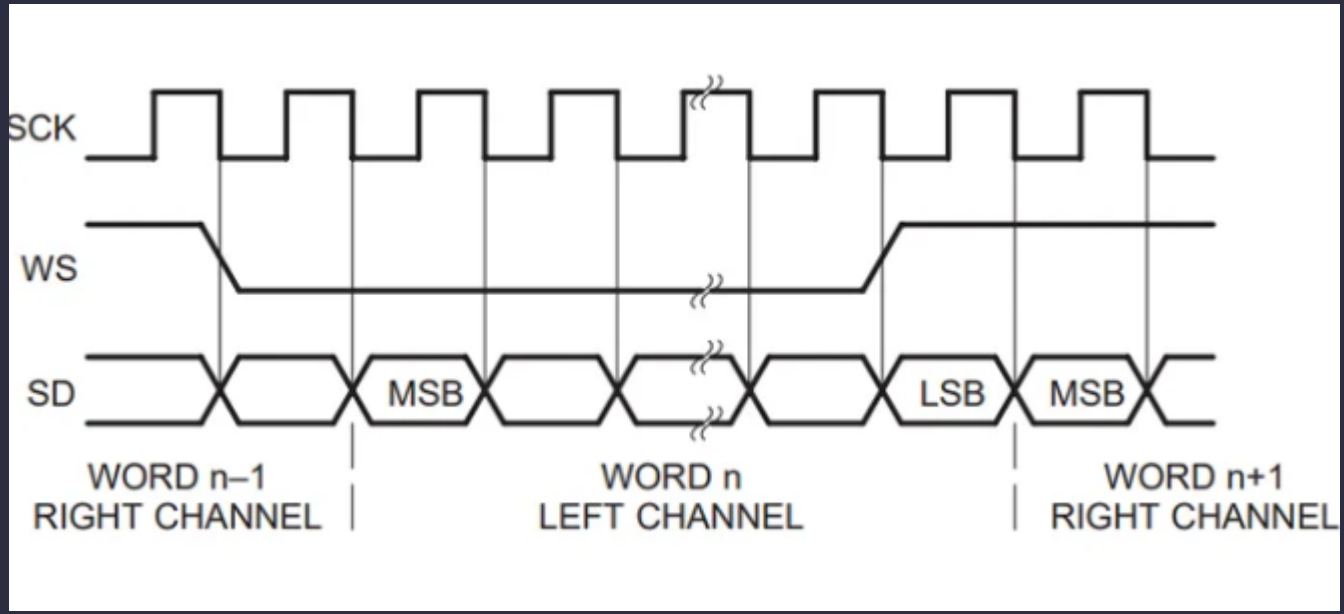
Feature	SPI	eCSPI
Basic Functionality	Standard SPI protocol	Extended SPI with enhanced features
FIFO (First-In-First-Out Buffer)	Typically lacks deep FIFO	Has up to 64-byte FIFO buffers
Slave Select (SS) Control	Master manually controls SS	Automatic SS control for multiple slaves
Chip Select Lines	Typically 1-2 SS lines	Supports up to 4 chip select (CS) lines
Data Transfer Size	Fixed (usually 8 or 16 bits)	Programmable word lengths (8-32 bits)
Baud Rate Control	Limited	More flexible and independent clock settings per channel
Loopback Mode	Not common	Supports internal loopback testing
Multi-Channel Support	Single SPI bus per instance	Multiple simultaneous SPI transfers via channels
DMA Support	Limited or requires CPU intervention	Better DMA support for high-speed transfers
Interrupt Handling	Basic interrupt system	More granular interrupt control

MCU & MPU Architectures, Interfaces

- Microprocessor Unit

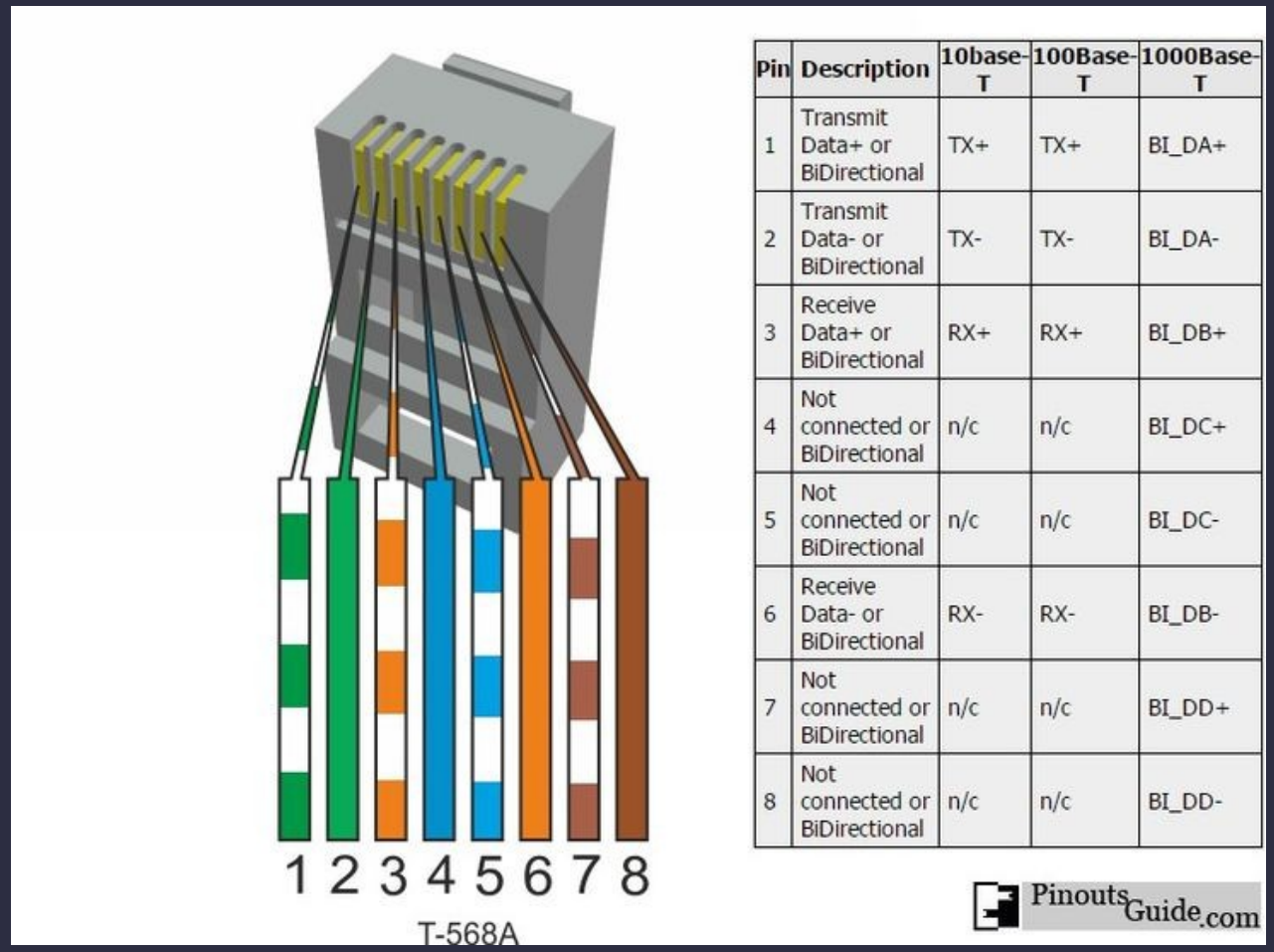
  - i.MX 6 Overview
  - MPU Blocks

  - SAI (Synchronous Audio Interface)
  - Supports
    - I2S (Inter IC Sound)
    - AC97
    - TDM



MCU & MPU Architectures, Interfaces

- Microprocessor Unit
  - i.MX 6 Overview
  - MPU Blocks
  - Ethernet



Pin	Description	10base-T	100Base-T	1000Base-T
1	Transmit Data+ or BiDirectional	TX+	TX+	BI_DA+
2	Transmit Data- or BiDirectional	TX-	TX-	BI_DA-
3	Receive Data+ or BiDirectional	RX+	RX+	BI_DB+
4	Not connected or BiDirectional	n/c	n/c	BI_DC+
5	Not connected or BiDirectional	n/c	n/c	BI_DC-
6	Receive Data- or BiDirectional	RX-	RX-	BI_DB-
7	Not connected or BiDirectional	n/c	n/c	BI_DD+
8	Not connected or BiDirectional	n/c	n/c	BI_DD-

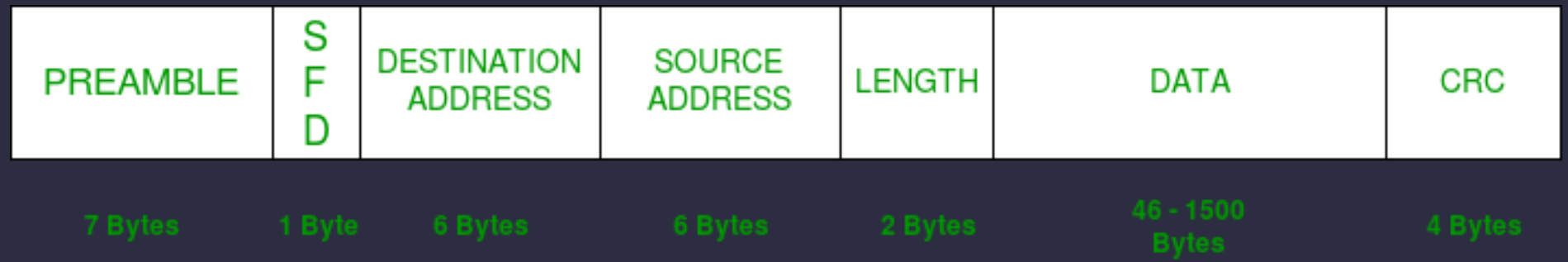
PinoutsGuide.com

MCU & MPU Architectures, Interfaces

- Microprocessor Unit

  - i.MX 6 Overview
  - MPU Blocks

  - Ethernet



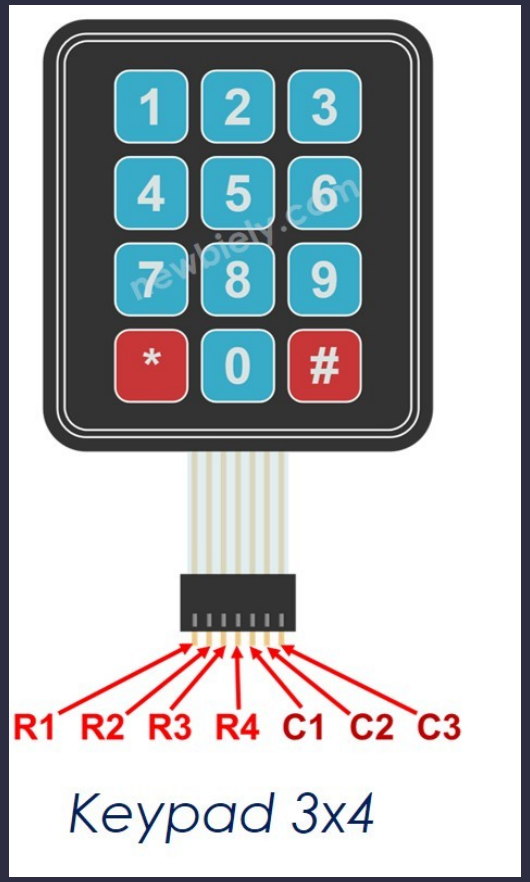
IEEE 802.3 ETHERNET Frame Format

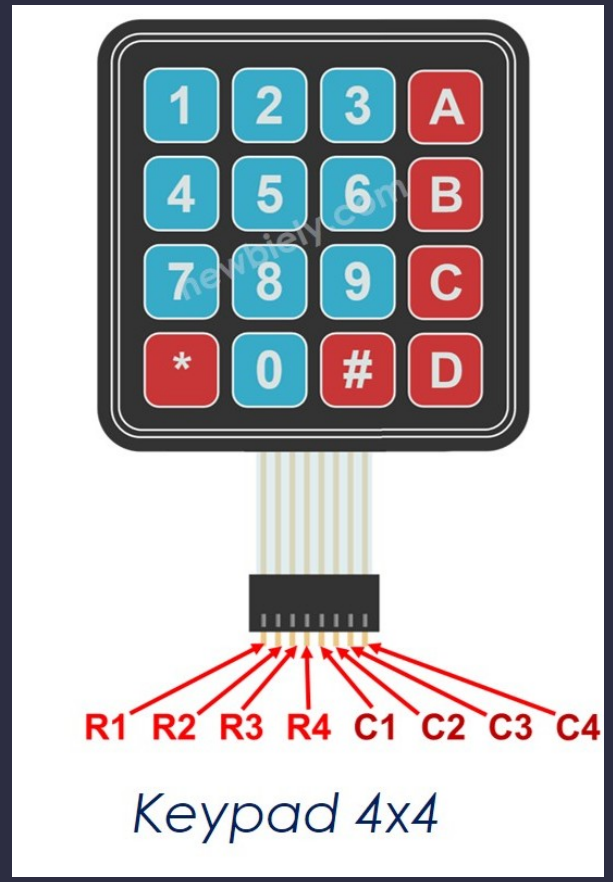
MCU & MPU Architectures, Interfaces

- Microprocessor Unit

  - i.MX 6 Overview
  - MPU Blocks

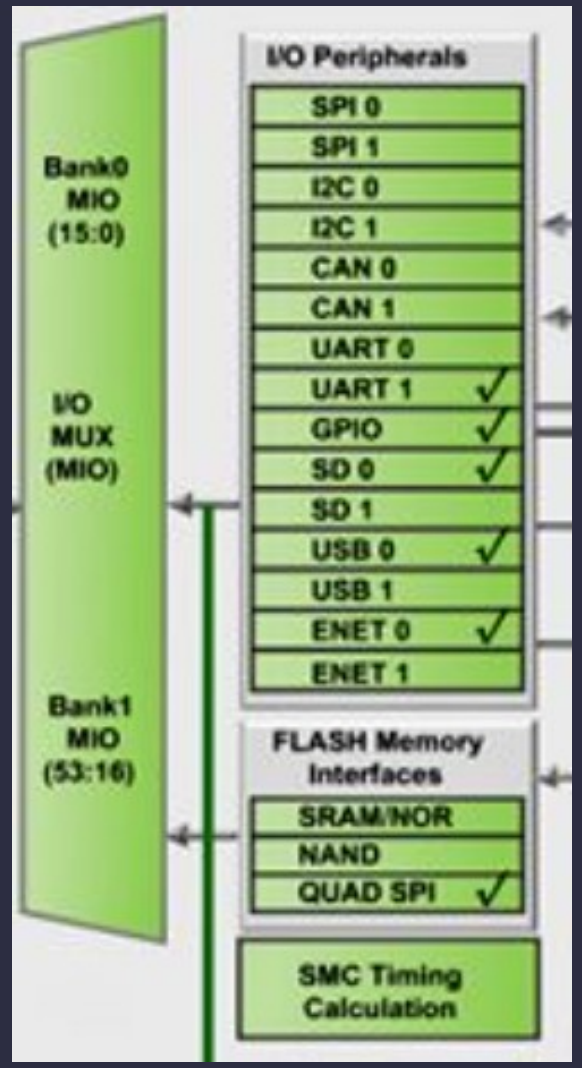
  - KPP (Keypad Port)





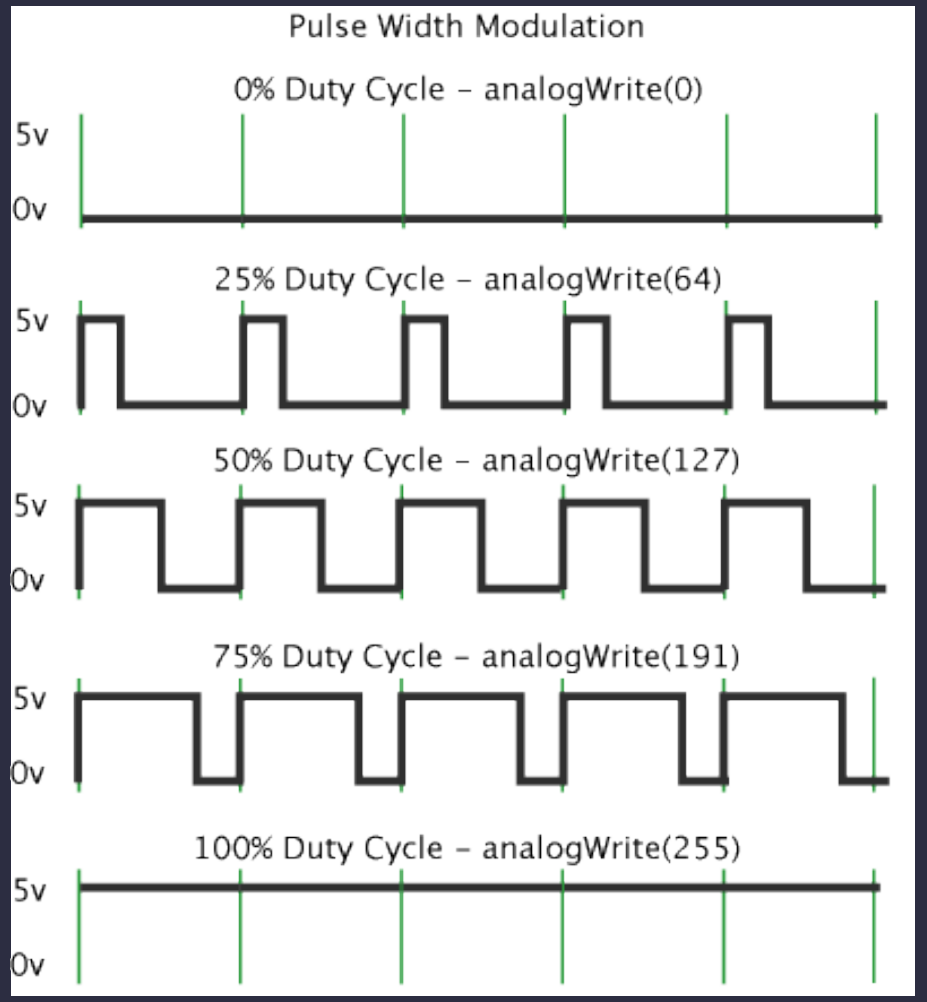
MCU & MPU Architectures, Interfaces

- Microprocessor Unit
  - i.MX 6 Overview
  - MPU Blocks
  - IOMUX



MCU & MPU Architectures, Interfaces

- Microprocessor Unit
  - i.MX 6 Overview
  - MPU Blocks
  - PWM

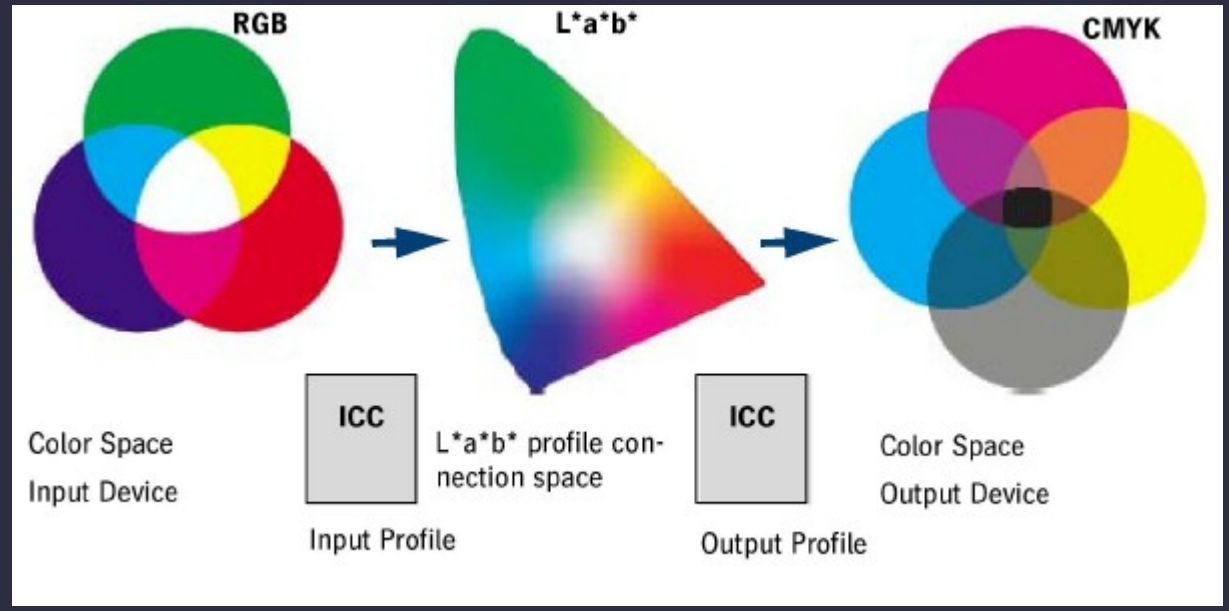


MCU & MPU Architectures, Interfaces

- Microprocessor Unit

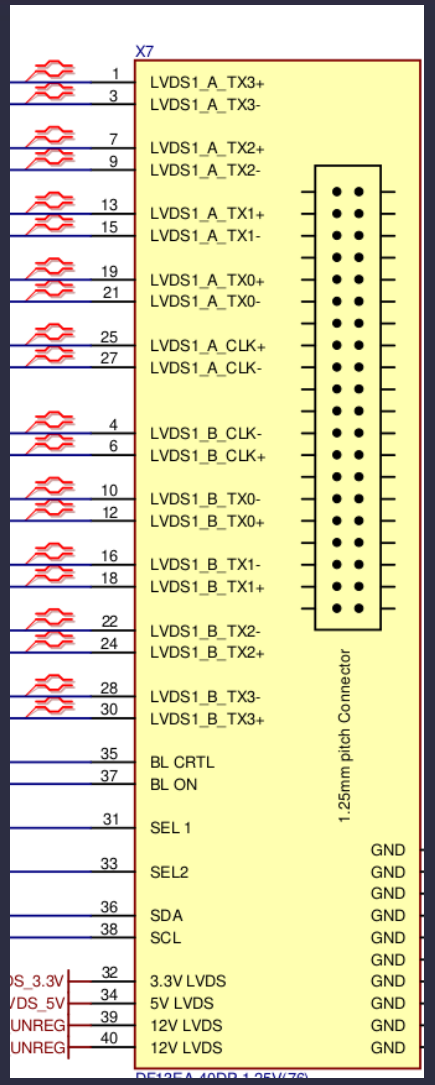
  - i.MX 6 Overview
  - MPU Blocks

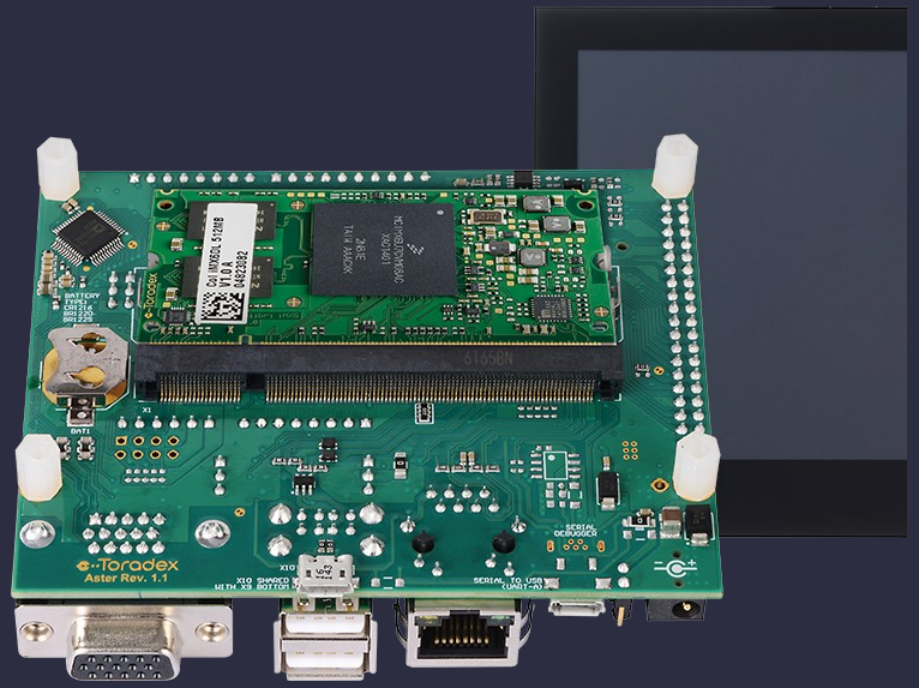
  - PXP (Pixel Processing Pipeline)
  - 2D Image Processing
    - Color Space Conversion
    - Scaling
    - Alpha Blending
    - Rotation



MCU & MPU Architectures, Interfaces

- Microprocessor Unit
  - i.MX 6 Overview
  - MPU Blocks
  - LCDIF





MCU & MPU Architectures, Interfaces

- Microprocessor Unit

  - i.MX 6 Overview
  - MPU Blocks

  - CSU (Central Security Unit)

  - The Central Security Unit (CSU) manages the system security policy for peripheral access on the SoC.

  - The CSU allows trusted code to set individual security access privileges on each of the peripherals, using one of the eight security access privilege levels

MCU & MPU Architectures, Interfaces

- Microprocessor Unit
- i.MX 6ULL vs STM32F401RE

Feature	i.MX 6ULL (NXP)	STM32F401RE (STMicroelectronics)
Type	Microprocessor (MPU)	Microcontroller (MCU)
Core	ARM Cortex-A7	ARM Cortex-M4
Clock Speed	Up to 900 MHz	84 MHz
Memory (RAM)	Up to 512MB DDR3L/LPDDR2 (External)	96 KB (Internal)
Flash Memory	Uses external NAND/eMMC	512 KB (Internal)
Operating Voltage	3.3V	3.3V
GPIOs	150+	50
Timers	Multiple (including watchdog, PWM, RTC)	10 (including advanced timers)
ADC	No built-in ADC	12-bit, 16 channels
DAC	No built-in DAC	12-bit, 2 channels
PWM	Yes, advanced	Yes, advanced
USB Support	USB 2.0 OTG, USB PHY	USB 2.0 Full-Speed
Ethernet	Yes (10/100 Mbps)	No
UART/I2C/SPI	8x UART, 4x I2C, 4x SPI	3x UART, 3x I2C, 3x SPI
External Memory Interface	Yes (DDR3, LPDDR2, NAND, NOR, eMMC)	No (only Flash/RAM)
Power Consumption	Higher (Linux-capable MPU)	Lower (Low-power MCU)
Development Tools	Yocto, Linux, FreeRTOS	STM32CubeIDE, Keil, IAR

Feature	i.MX 6ULL	STM32F401RE
Processing Power	✅ Much faster (900 MHz)	❌ Slower (84 MHz)
Operating System	✅ Runs Linux	❌ No OS (bare-metal or RTOS)
Memory & Storage	✅ Supports external RAM & storage	❌ Limited internal RAM & Flash
Real-Time Processing	❌ Not optimized for real-time tasks	✅ Excellent for real-time applications
Power Efficiency	❌ Higher power consumption	✅ Lower power consumption
Connectivity	✅ Ethernet, USB OTG, WiFi support	❌ No Ethernet, USB Full-Speed only
GPIO Count	✅ More GPIOs (150+)	❌ Fewer GPIOs (50)
Embedded Peripherals	❌ No ADC/DAC	✅ 12-bit ADC/DAC