



Istanbul Technical University

CEN 242E – Logical Circuits Lab

LAB 1: Combinational Circuits

About LAB:

Introduction to Verilog Language, designing combinational circuits

Stages and scores of LAB :

1- Simple Calculator

A module called testModule will be developed. The input and output signals of the module are given as follows.

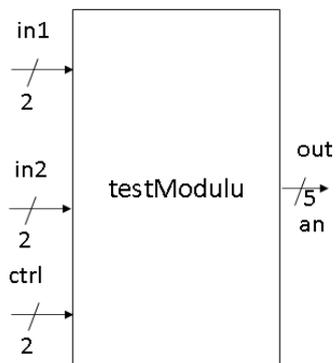


Figure. Test Module Inputs Outputs

This module produces output from the out port by performing arithmetic operations with in1 and in2 according to the value of the ctrl input.

- if ctrl == 0, out = in1 + in2
- If ctrl == 1, out = in1 – in2
- If ctrl == 2, out = in1 * in2
- Else, out = 5'b11111

2- Design the below circuit with verilog language

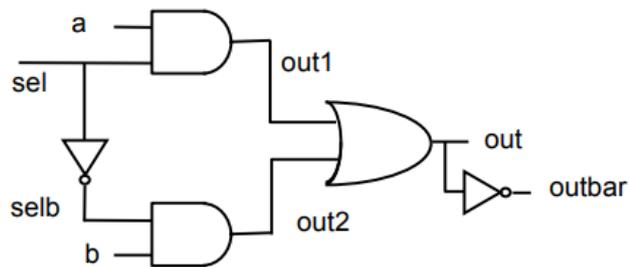


Figure. Reference Design

3- Design a decoder with 3 bits of input and outputs 8 bits of output.

Example 2-bit decoder :

```

`timescale 1ns / 1ps

module testModulu ( input [1:0] in , output reg [2:0] out );

    always @(*) begin
        if (in ==0)
            out = 4'b0001;
        else if (in == 1)
            out = 4'b0010;
        else if (in == 2)
            out = 4'b0100;
        else if (in == 3)
            out = 4'b1000;
        end
    endmodule

```

4- SevenSegment Driver

The figure shows the inputs and outputs of the SevenSegment design.

The output named 'an' drives 8 lamps of the seven segment. The seven segment operates as an anode, meaning it is active when supplied with 0.

Design the system by considering the required values for the lamps based on the numbers between 0 and 7 supplied from the 'sw' input.

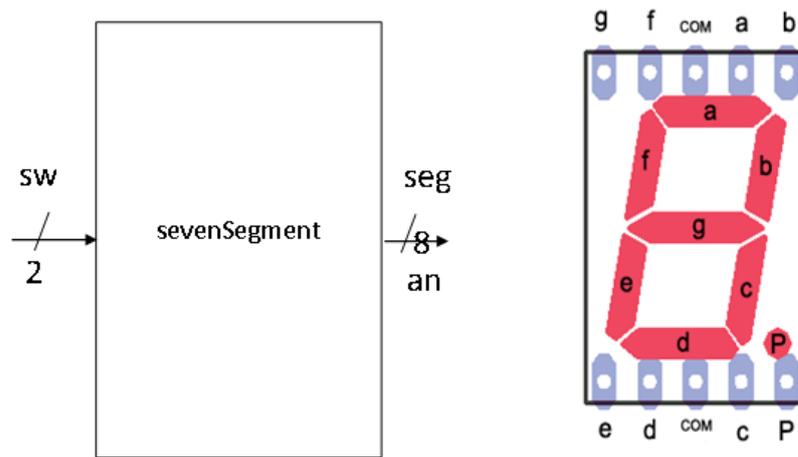


Figure. Seven Segment