İstanbul Technical University

CEN 242E – Logical Circuits Lab

LAB 2: Sequential Circuits

About LAB:

Introduction to Verilog Language, designing combinational circuits

Stages and scores of LAB :

1- LED Blinking

Design a Verilog module to make an LED blink such that it stays on for 1 second and off for 1 second in each cycle.

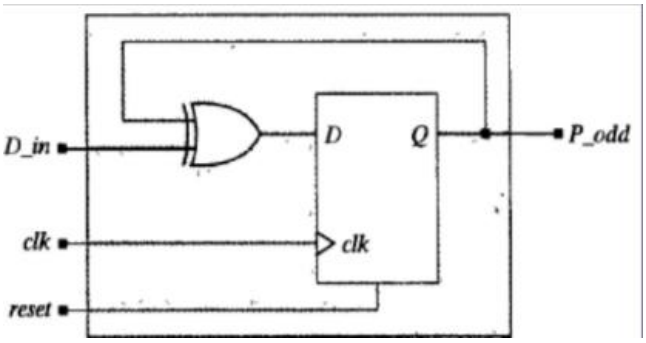
The module will receive a clock signal with a frequency of 10 Hz as input.

Use this clock to generate the necessary timing for the LED to follow the described behavior.

2- Adder

Design a Verilog module that receives a 4-bit input number and has a button input.
The module should include an internal register initialized to 0.
Each time the button is pressed, the module should add the 4-bit input number to the value stored in the register.
The result should be output as a 5-bit number. Ensure the module handles the button press correctly to avoid unintended multiple additions due to button bounce.

3- Write the Verilog representation of the circuit given.



4- LED Control

Design a Verilog module with two button inputs (button1 and button2) and two LED outputs (led1 and led2).

The behavior of the module should be as follows:

- When button1 is pressed and released, the state of led1 toggles. If led1 is on, it turns off, and if it is off, it turns on.
- When button2 is pressed, the state of led2 toggles. If led2 is off, it turns on, and if it is on, it turns off.

The module should include internal registers to maintain the state of the LEDs and ensure that button presses are handled correctly to avoid unintended toggles due to button bounce.

5- LED Manager

Design a Verilog module named ledManager with the following specifications:

1. **Inputs**:
    - clk: A 1-bit clock signal.
    - rst: A 1-bit reset signal.
1. **Output**:
    - LED: A 16-bit output signal representing the state of 16 LEDs.
1. **Functionality**:

- When the rst signal is active, the LED output should reset to 16'b1000000000000000, where only the leftmost LED is on, and all others are off.
- When the rst signal is inactive, the LED output should shift one position to the right on each clock cycle, creating a rotating LED effect. After the rightmost LED is turned on, the sequence should restart with the leftmost LED on.

Note: Since the FPGA clock operates at 10 Hz, the shifting pattern will appear very fast to the human eye. To make the movement visible, consider adding a clock divider circuit to slow down the LED transitions.