İstanbul Technical University

CEN 242E – Logical Circuits Lab

LAB 3: Sequential Circuits II

About LAB:

Introduction to Verilog Language, designing combinational circuits

Stages and scores of LAB :

1- Debounced Counter

Design a 4-bit counter system controlled by push buttons.

Requirements

Input	Function
BTN0	Increment counter
BTN1	Decrement counter

Counter range:

0 → 15

The counter value must be displayed on a seven-segment display.

Important

Push buttons must be debounced before they are used.

Output

HEX0 → Counter value

2- LED Pattern Generator

Create a programmable LED pattern engine.

Switch Functions

Switch	Function
SW0	Enable pattern generator
SW2:SW1	Pattern selection

Patterns

Mode 0 — Running LED

0001 → 0010 → 0100 → 1000

Mode 1 — Ping-Pong

0001 → 0010 → 0100 → 1000 → 0100 → 0010

Mode 2 — Rotate

Mode 3 — Flash all LEDs

Output

LED[3:0]

3- Stopwatch with Lap

Implement a **digital stopwatch**.

Buttons

Button	**Function**
BTN0	Start
BTN1	Stop
BTN2	Lap
BTN3	Reset

Requirements

- Internal **millisecond counter**
- Display time on **seven segment display**
- Lap should **freeze display while timer continues internally**

4- Up/Down Speed Controlled Counter

Description

Design a speed-controlled up/down counter using switches.

Inputs

Input	Function
BTN0	Count enable
SW0	Direction (0 = Up, 1 = Down)
SW2:SW1	Speed select

Speed Modes

SW2 SW1	Speed
00	Slow
01	Medium
10	Fast
11	Very Fast

Speed must be implemented using a clock divider.

Counter

8-bit counter

0 → 255

Output

Output	Function
LED[7:0]	Counter value