



Istanbul Technical University

CEN 242E – Logical Circuits Lab

LAB 4: State Machines

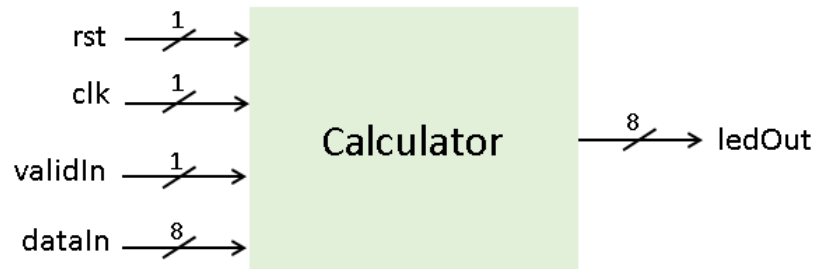
About LAB:

Introduction to Verilog Language, designing combinational circuits

Stages and scores of LAB :

1- Calculator

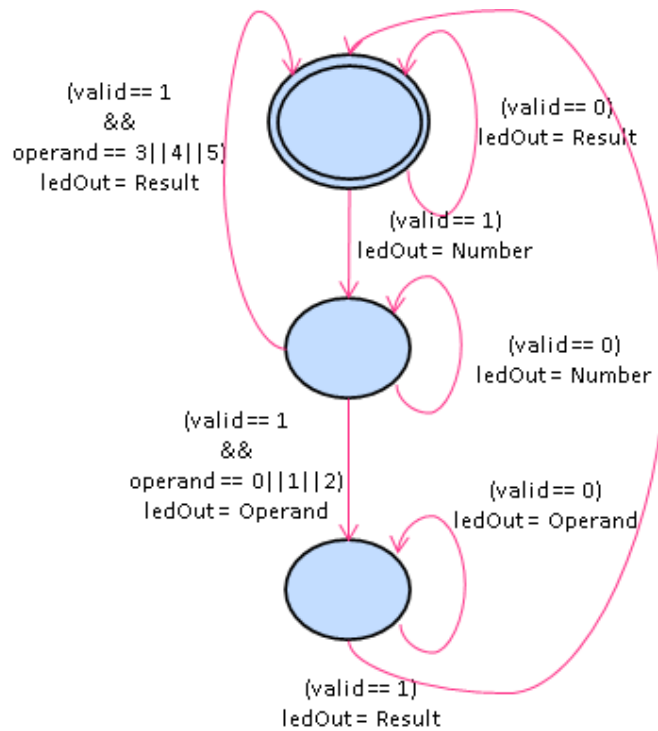
It is desired to design a simple calculator with the state machine methodology. The inputs and outputs of the module are given as follows. When a 1 signal is given from the valid port, the design work will be carried out as the value given from the dataIn signal is valid.



This calculator can perform 6 operations. These are;

- Multiplication
- Addition
- Subtraction
- Square
- One add
- One subtract

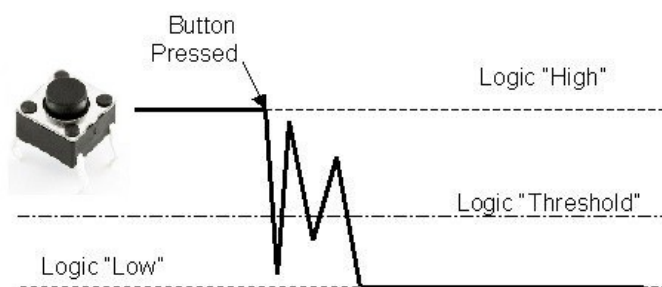
The first 3 operations require two numbers. The last three numbers can be processed with a single number. The state machine representation of the design is given below. The calculation process is completed in 2 or 3 stages.



Make a Verilog RTL design according to the given diagram and configure it to the FPGA. Use buttons for ValidIn, switches for dataIn and LEDs for the output signal.

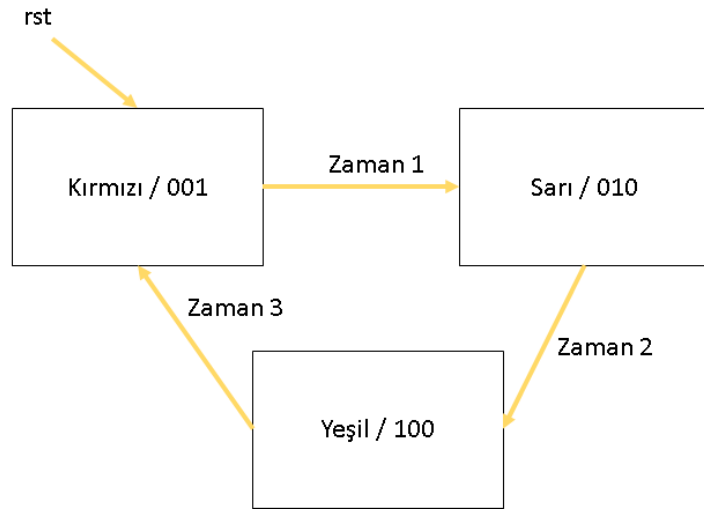
Note: Pay attention to the debouncing status.

Button "Bounce"



2- Traffic Light Controller

A state machine design will be made for traffic lights. The state machine will have 3 states. The diagram of the state machine is given below.



The design will switch to the state where the red lamp is turned on when the reset button is pressed. If the reset button is not pressed, it will remain in the red state for 5 seconds, in the yellow state for 0.5 seconds, and in the green state for 2 seconds. The Red -> Yellow -> Green -> Red ... cycle will be repeated.

Use 3 different LEDs for Red, Yellow and Green displays. Make a verilog display of the design and configure it to the FPGA.