İstanbul Technical University

CEN 242E – Logical Circuits Lab

LAB 7: Verification II

About LAB:

Verification II

Stages and scores of LAB :

1- Buggy Multiplication Module

You have a 5×5-bit multiplier module, **buggyMultiplier**, that intentionally produces incorrect results for exactly 13 specific input pairs. Write a Verilog testbench module named **tb_buggyMultiplier** which:

1. Declares two 5-bit reg inputs (in1, in2) and a 10-bit wire output (out).
2. Instantiates **buggyMultiplier** without modifying it.
3. Uses nested loops (over integer loop counters) to drive every possible 5-bit combination on in1/in2, waiting exactly 1 ns after each assignment.
4. On each cycle, computes the true product (in1 * in2) and, if it doesn't match the DUT's out, increments a 16-bit reg called error_count.
5. Leaves error_count holding the total number of mismatches once all 32×32 cases have been tested.

Do not include any $display or $error or $finish statements in your testbench—its sole job is to exercise the DUT and tally the failures into error_count.

2- Broken Traffic Light

You have a **faulty trafficLight hardware module** whose outputs (RED, YELLOW, GREEN) should normally light in sequence, but at some point **all three LEDs turn on simultaneously**.

Your task is to write a Verilog testbench that:

1. Instantiates the trafficLight DUT.
2. Generates a 10 ns clock (always #5 clk = ~clk;).
3. Asserts rst for one clock cycle and then deasserts it.
4. Uses a “tur” counter (cycle_count) that increments on each rising edge of RED.
5. Monitors for the first time that RED && YELLOW && GREEN is true:
    - Sets a reg failure_seen flag to 1.
    - Captures the current cycle_count into an integer failure_cycle.
    - Exits the loop immediately.
6. Stops searching after a maximum of 7 red cycles if no failure is seen.

Use the following registers in your testbench:

reg failure_seen = 0;

integer failure_cycle = -1;

Write the complete testbench (without highlighting) that implements this logic and records in which “tur” the simultaneous-ON failure occurs.