SOC Design

Week 1: Introduction

Fenerbahçe University

Professor & TAs

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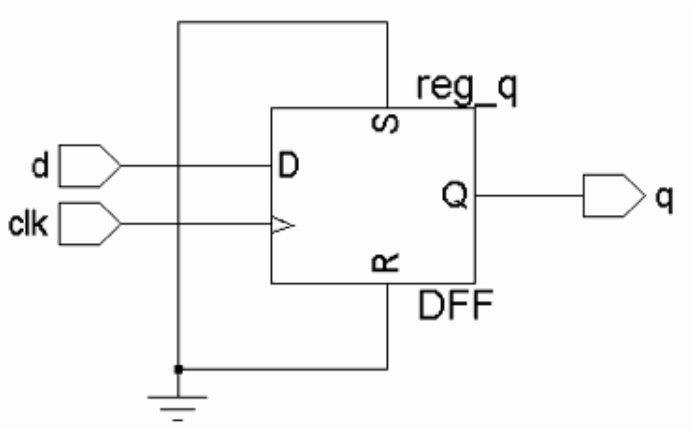
Course Plan

- System on Chip (SOC) Design
  - Introduction
  - RTL Design
  - ZYNQ Architecture
  - Datapaths (AXI Bus)
  - Interfaces I
  - Interfaces II
  - Interrupt’s
  - Microblaze I
  - Microblaze II
  - PL/PS CoProcessing
  - Hardware Accelerator
  - Performance Profiling and Debugging
  - QEMU

Course Plan

- RTL Design

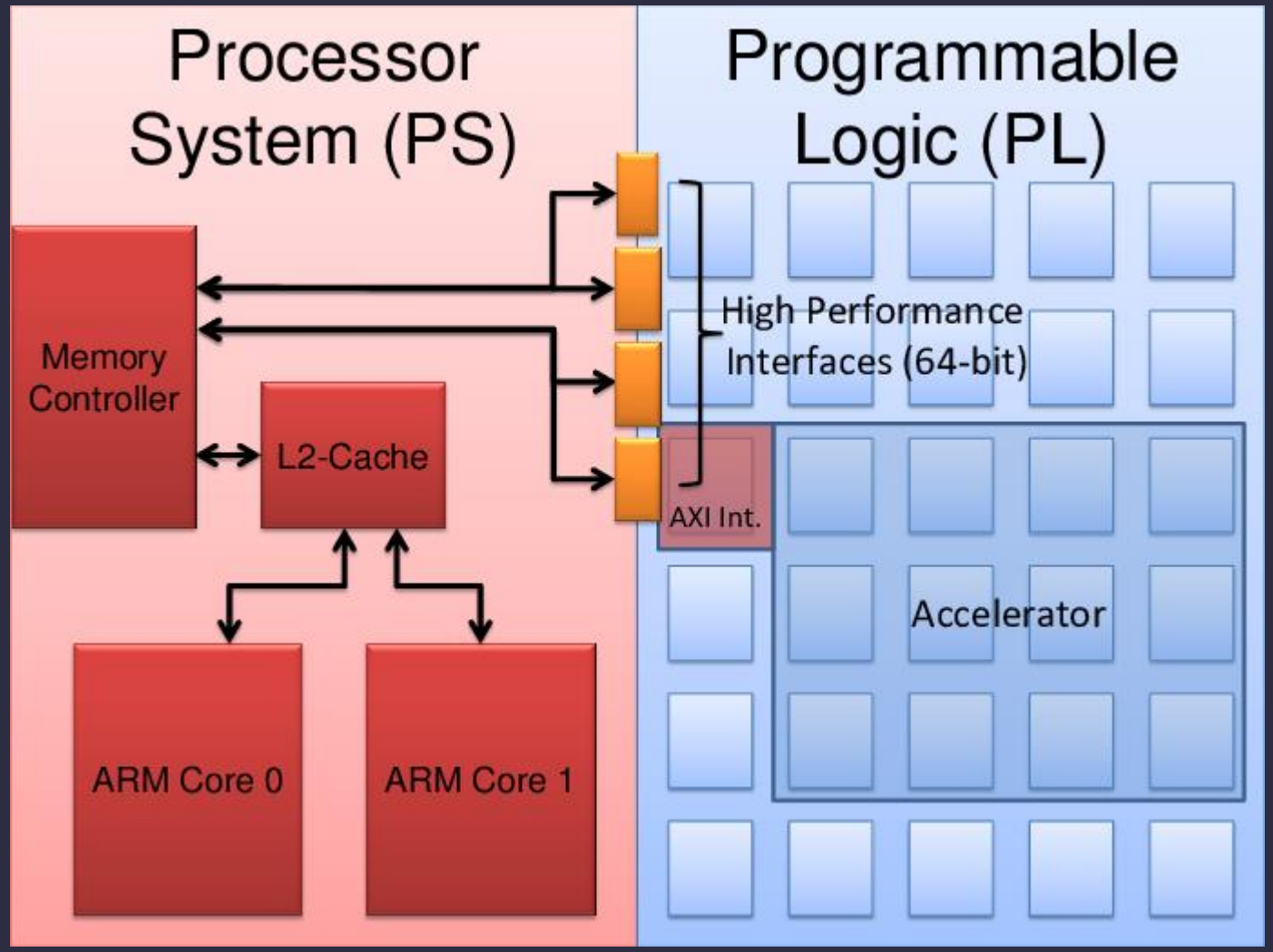
```
15      ff_proc: process (clk)
16      begin
17        if (clk = '1' and clk'event) then
18          q <= d;
19        end if;
20      end process ff_proc;
```




```
1   module ff (output reg q, input d,
2              input clk);
3
4     always @(posedge clk)
5       q <= d;
6
7   endmodule
```

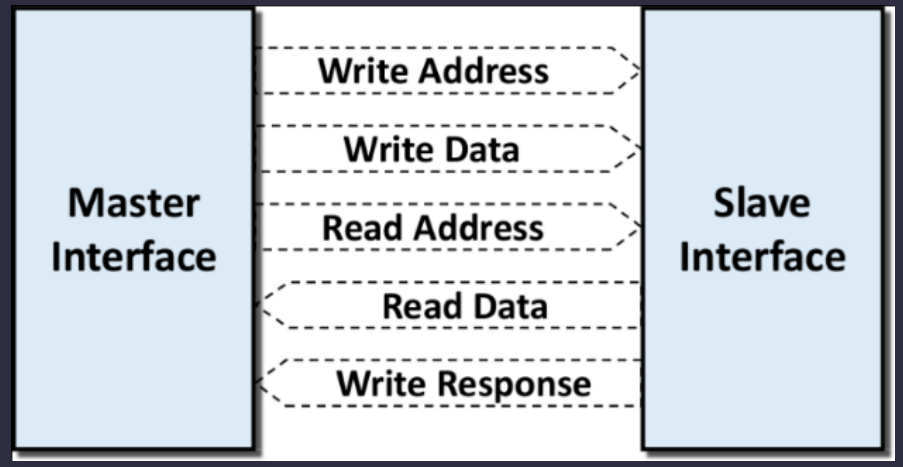
Course Plan

- ZYNQ Architecture

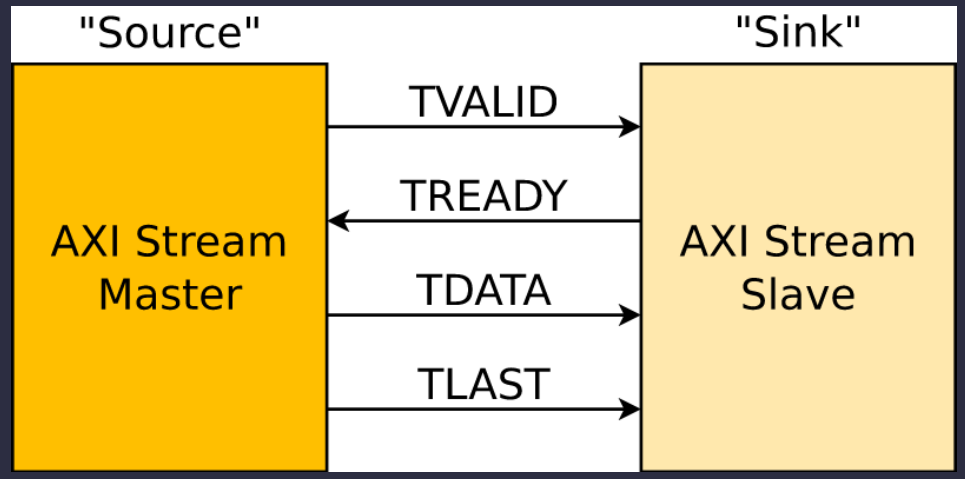


Course Plan

- Datapath



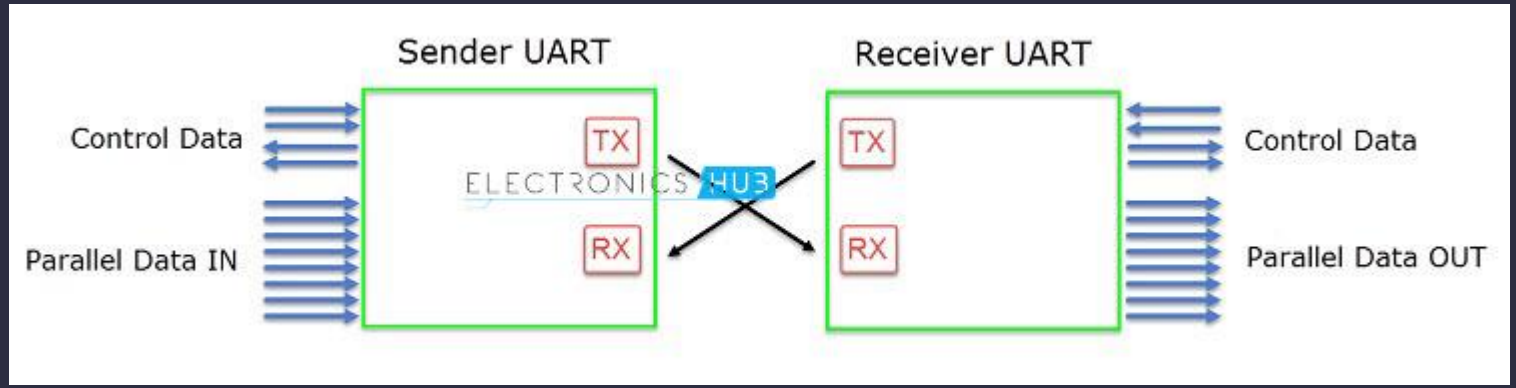
AXI MM

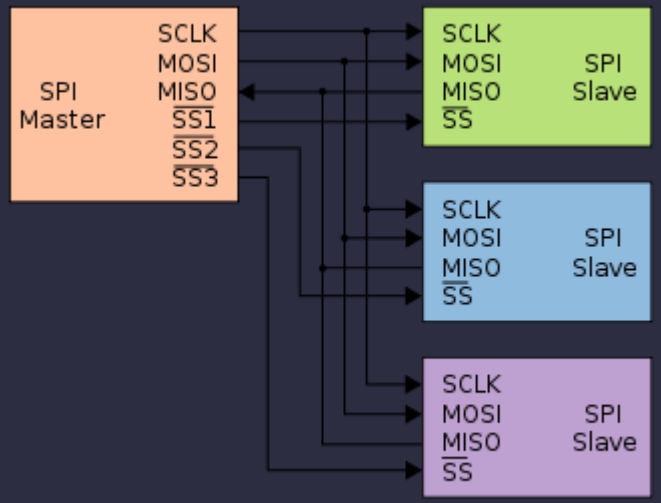


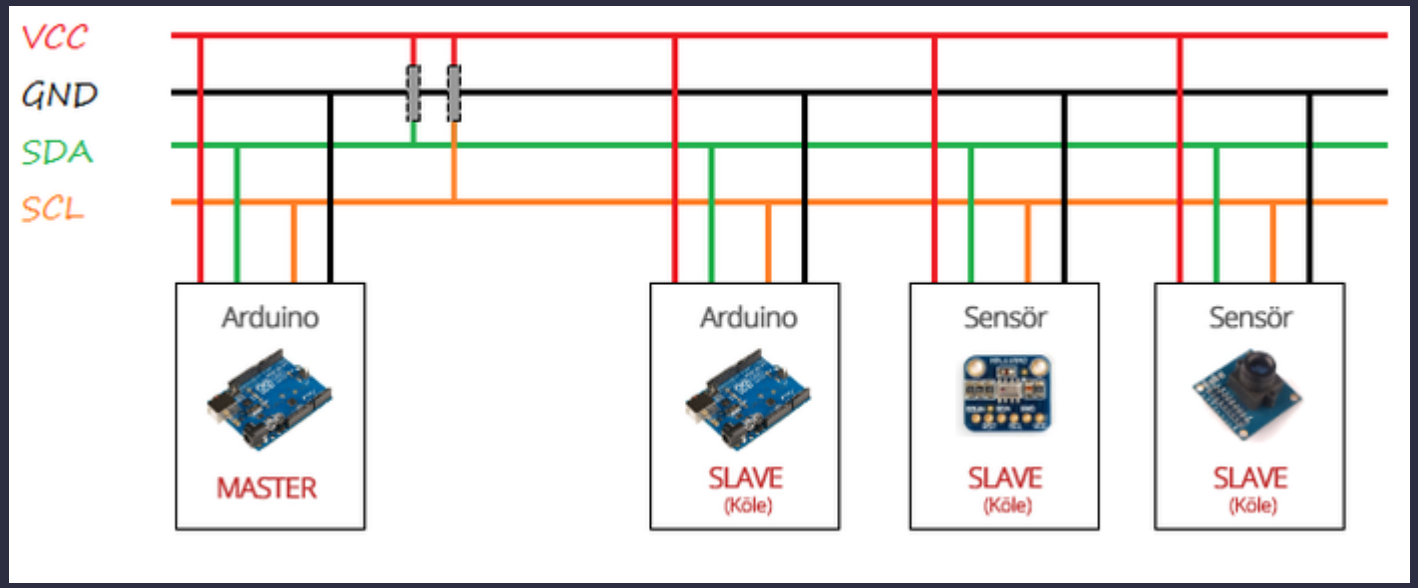
AXI Streaming

Course Plan

- Interfaces I

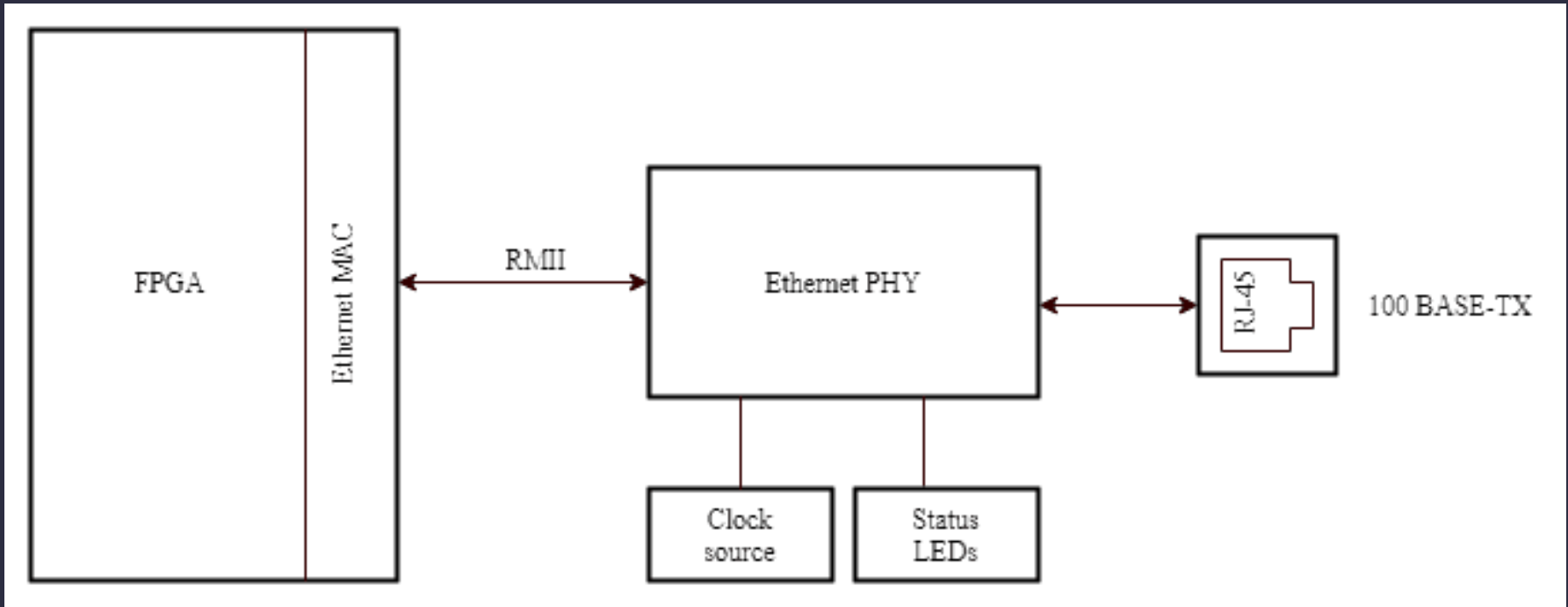






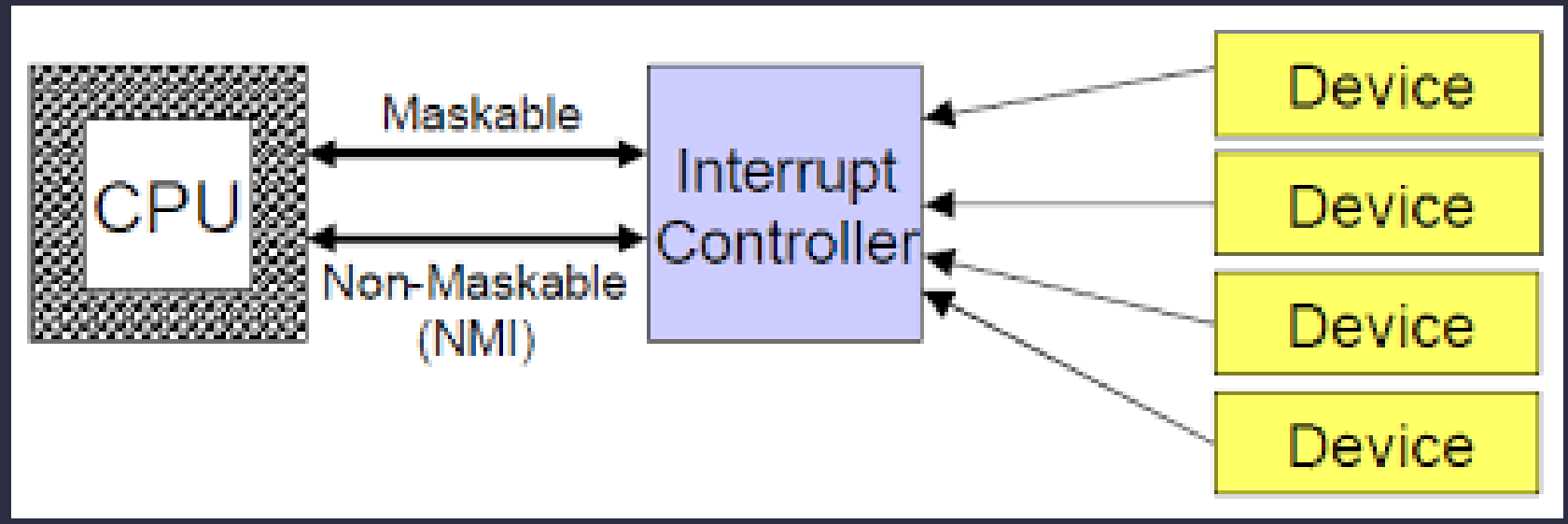
Course Plan

- Interfaces II



Course Plan

- Interrupts



Course Plan

- Microblaze I

Memory Access, GPIO Control

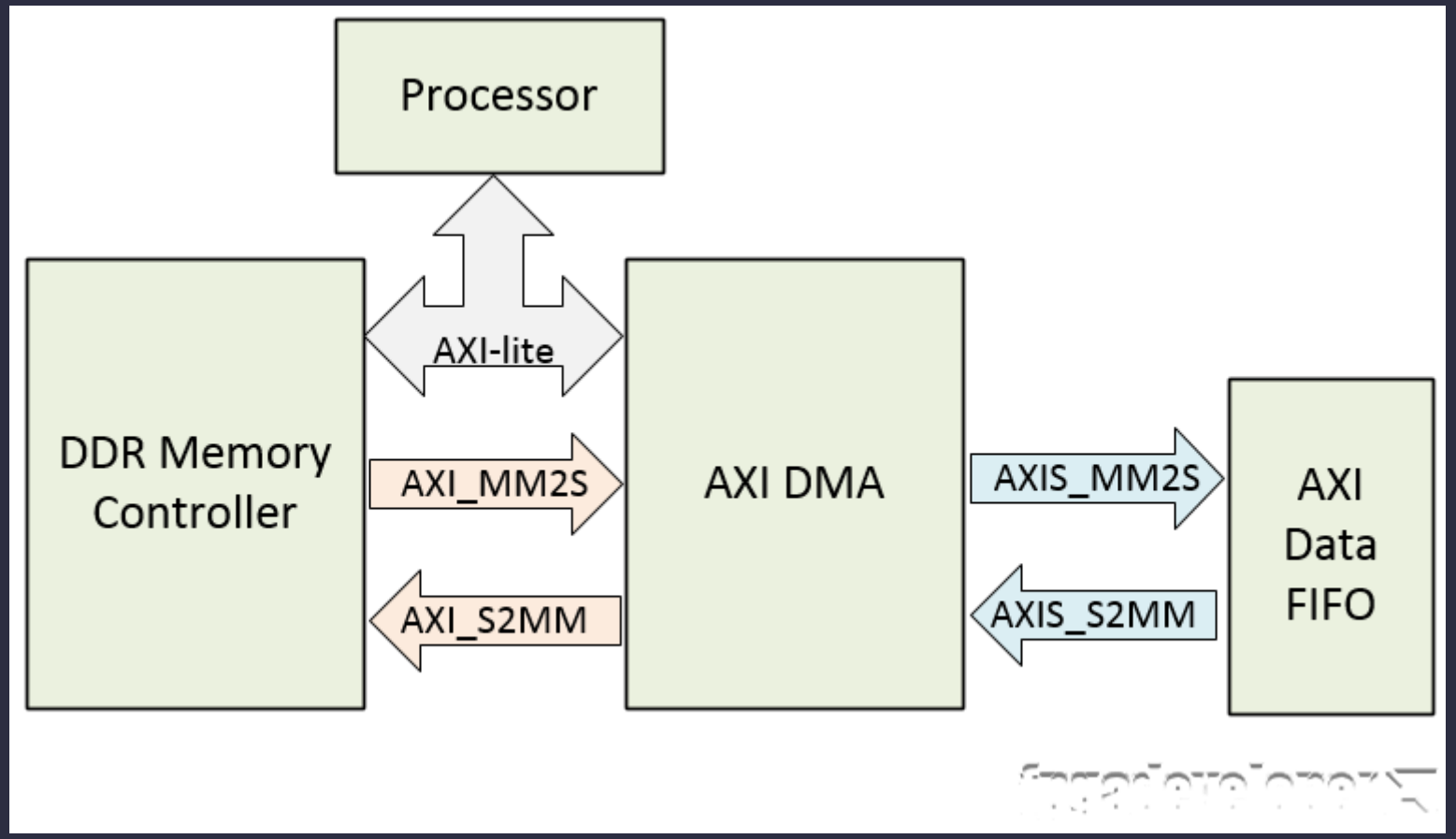
Course Plan

- Microblaze II

UART IP Integration

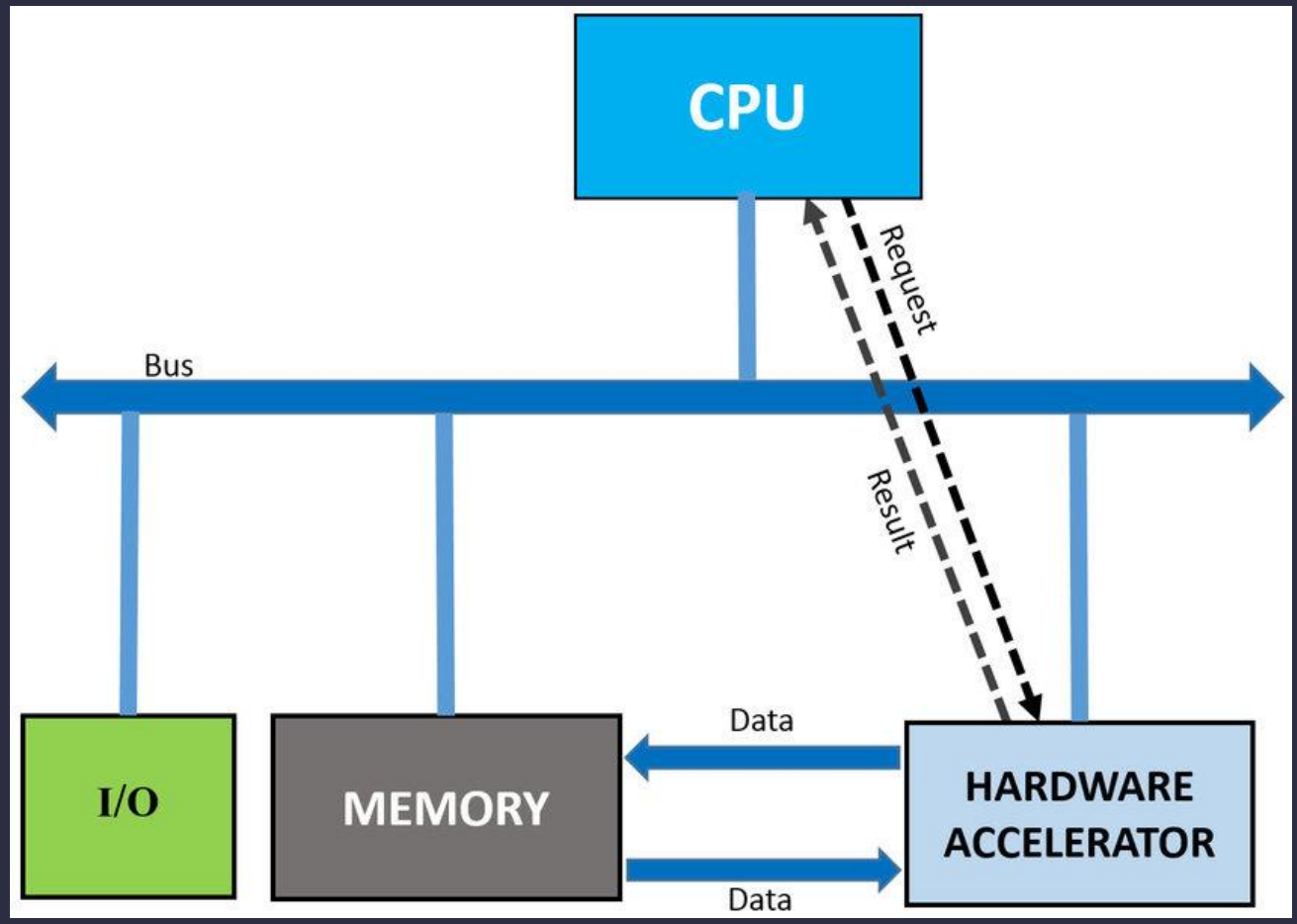
Course Plan

- PL/PS CoProcessing



Course Plan

- Hardware Accelerator

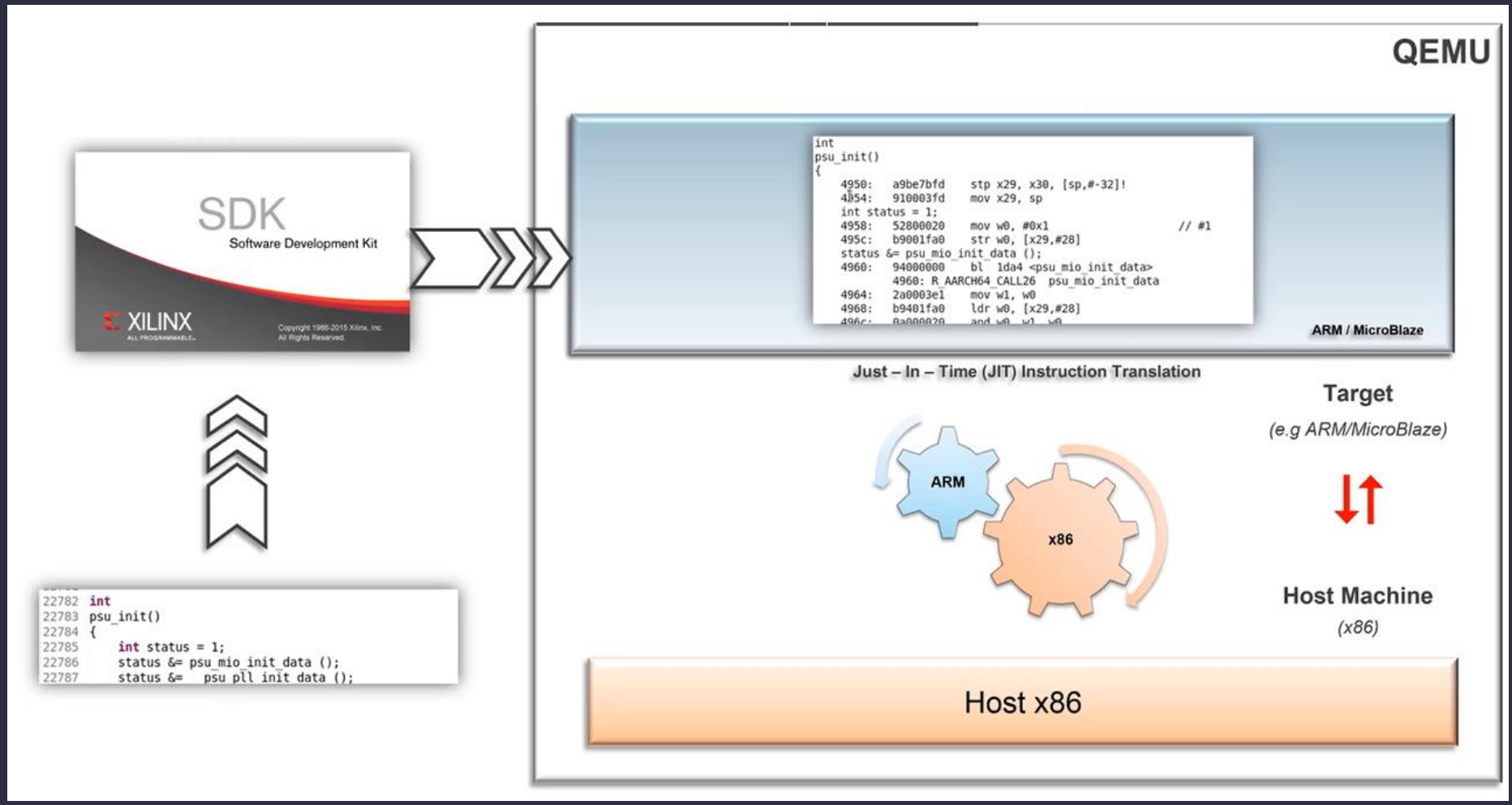


Course Plan

- Performance Profiling and Debugging

Course Plan

- QEMU



Course Contents

Website: levent.tc

Courses> SOC Design

Course Contents

Course Page Content;

- Syllabus
- Course Schedule
- Course Notes
- Homeworks
- Projects
- Exams
- LMS and Piazza
- Notes
- Feedback

Course Contents

Syllabus;

Lesson hours;

Monday 9.00-13.00

Office Hours;

Dr. Vecdi Emre Levent - Thursday 15.00-17.00

Assistant. Ezgi Çakmak - Tuesday 16.00-17.00, Friday 16.00-17.00

Course Contents

Syllabus;

Between 4-6 homework will be given.

2 Quizzes will be held.

Class attendance is compulsory at a rate of 80%.

Course Contents

Evaluation weights

Delivery time for assignments and quizzes
for every passing hour
5 points will be deducted.

Activities	Percentages
Midterm	%20
Homework / Quiz	%10
Lab	%15
Projets	%30
Final	%25
Bonus	Up to 5 points

Course Contents

Syllabus;

Grades

Point	Weight	Letter Grade
90-100	4.00	AA
85-89	3.50	BA
80-84	3.00	BB
75-79	2.50	CB
65-74	2.00	CC
50-64	1.50	DC
45-49	1.00	DD
0 -44	0	FF

Course Contents

Syllabus;

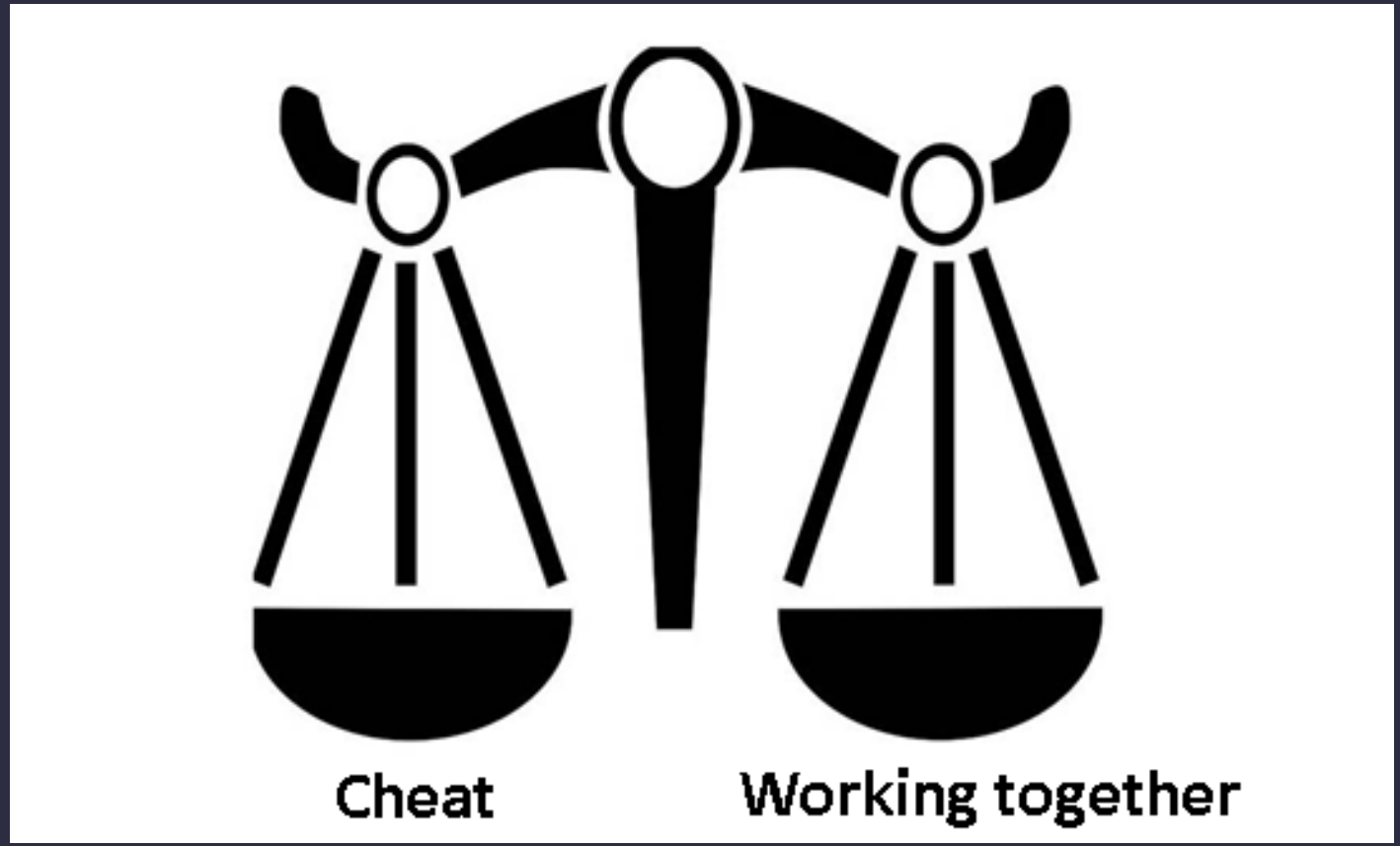
Expected effort

190 hours in total effort is expected.

Counnt	Hour	#Times	Total
Preparation	2	14	28
Repetition	2	14	28
Homeworks	4	6	24
Project	48	1	48
Course	4	14	56
Midterm and Finals	3	2	6

Course Contents

Academic honesty



Course Contents

Course schedule

Course Contents

Homeworks;

The assignments to be given and their solutions will be shared on the homework page.

Course Contents

Projects;

Projects to be completed by each student will be announced at the end of the term.

Course Contents

Exams;

Sample questions and solutions of exams will be shared for midterm and final exams.

Course Contents

LMS and Piazza;

The LMS system is the system where we will request some assignments to be uploaded. The system will automatically closed on the last upload date.

The Piazza system is a classroom question and answer platform. Whenever you have a topic about lecture, homework or exams, you can write on this platform. The questions you write are seen by teachers and students. You can also help each other measuredly through this platform.

Course Contents

Grades;

On the Grades page, all the grades you have collected in the course are given.

You can see how many points you have collected from midterm, homework, quiz, lab, final and bonuses by browsing through the pages.

Course Contents

Feedback,

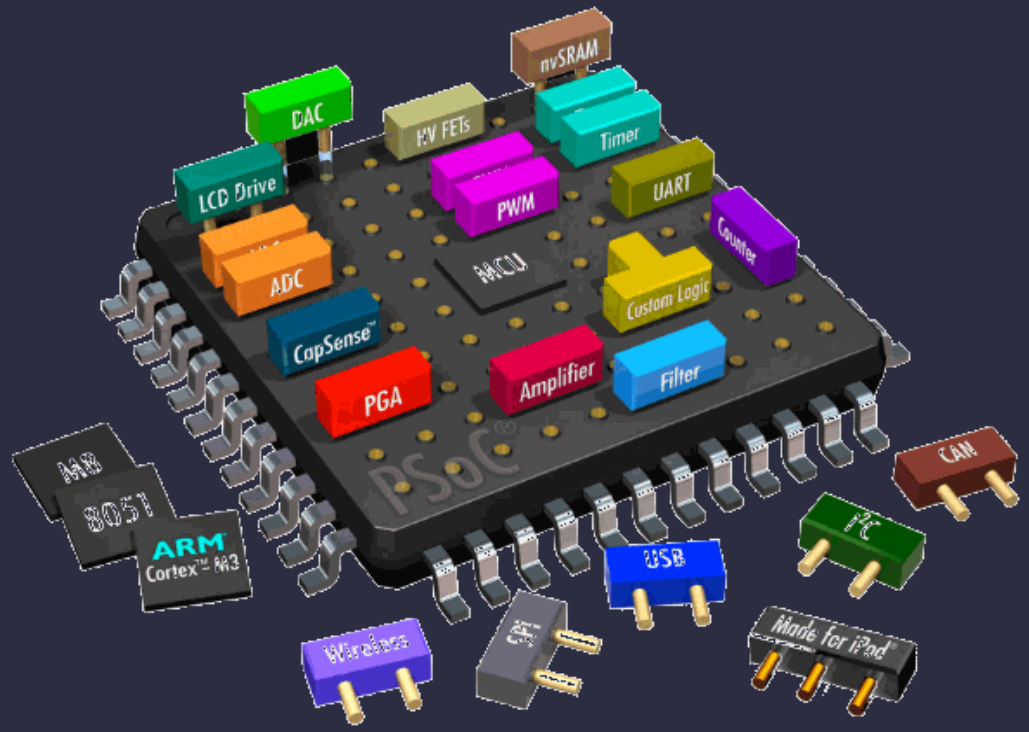
Feedback is very important for improving the quality of the lesson.

You can comment on the feedback mechanism that will be created every week through the LMS system.

Each time you make a comment, an additional 0.5 bonus points will be given to your end of year score.

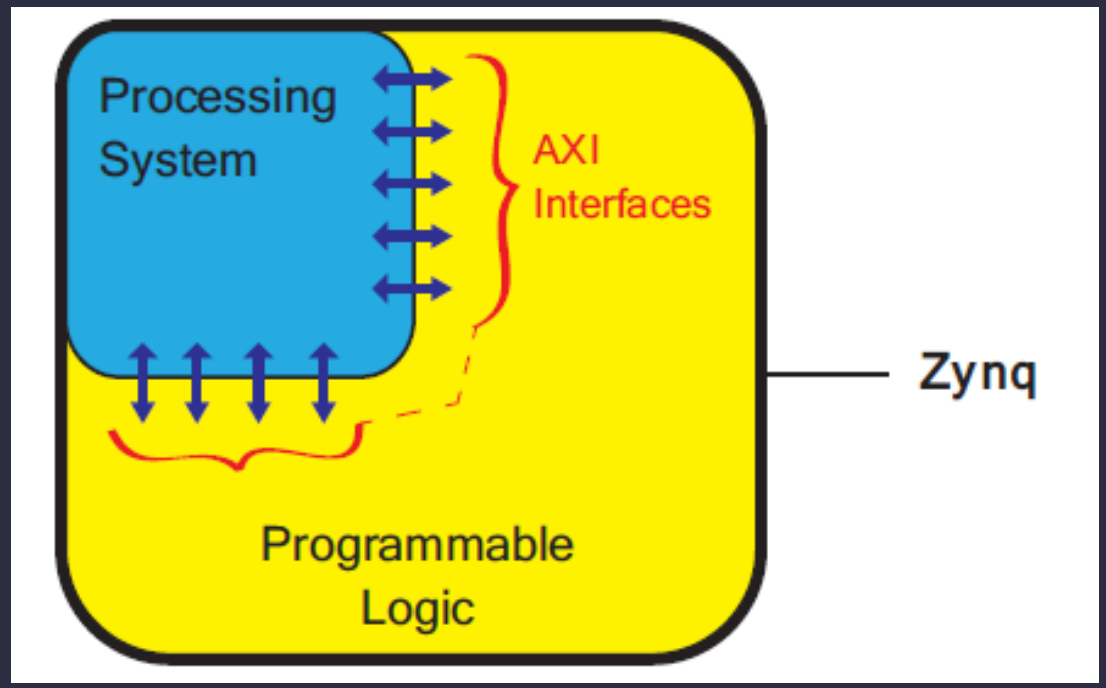
You can collect a maximum of 5 points bonus.

System on Chip (SOC) Design



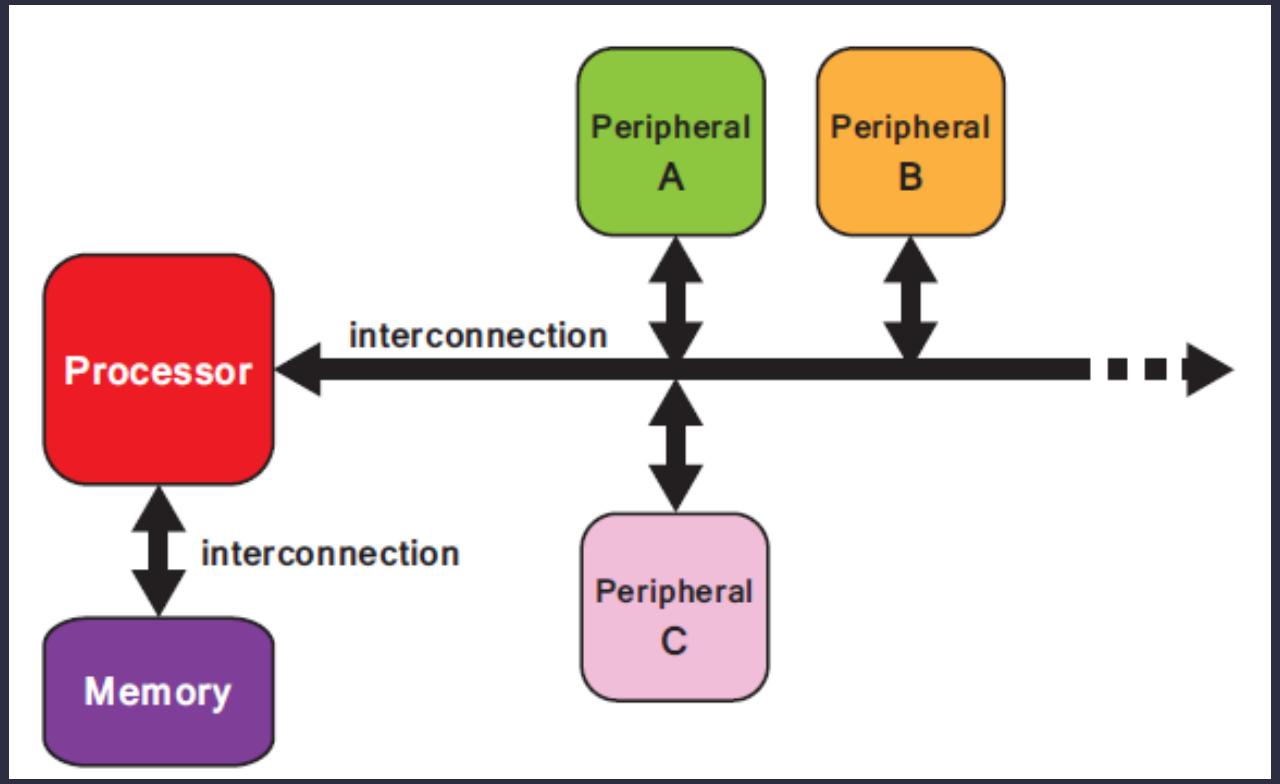
System on Board vs System on Chip

System on Chip (SOC) Design



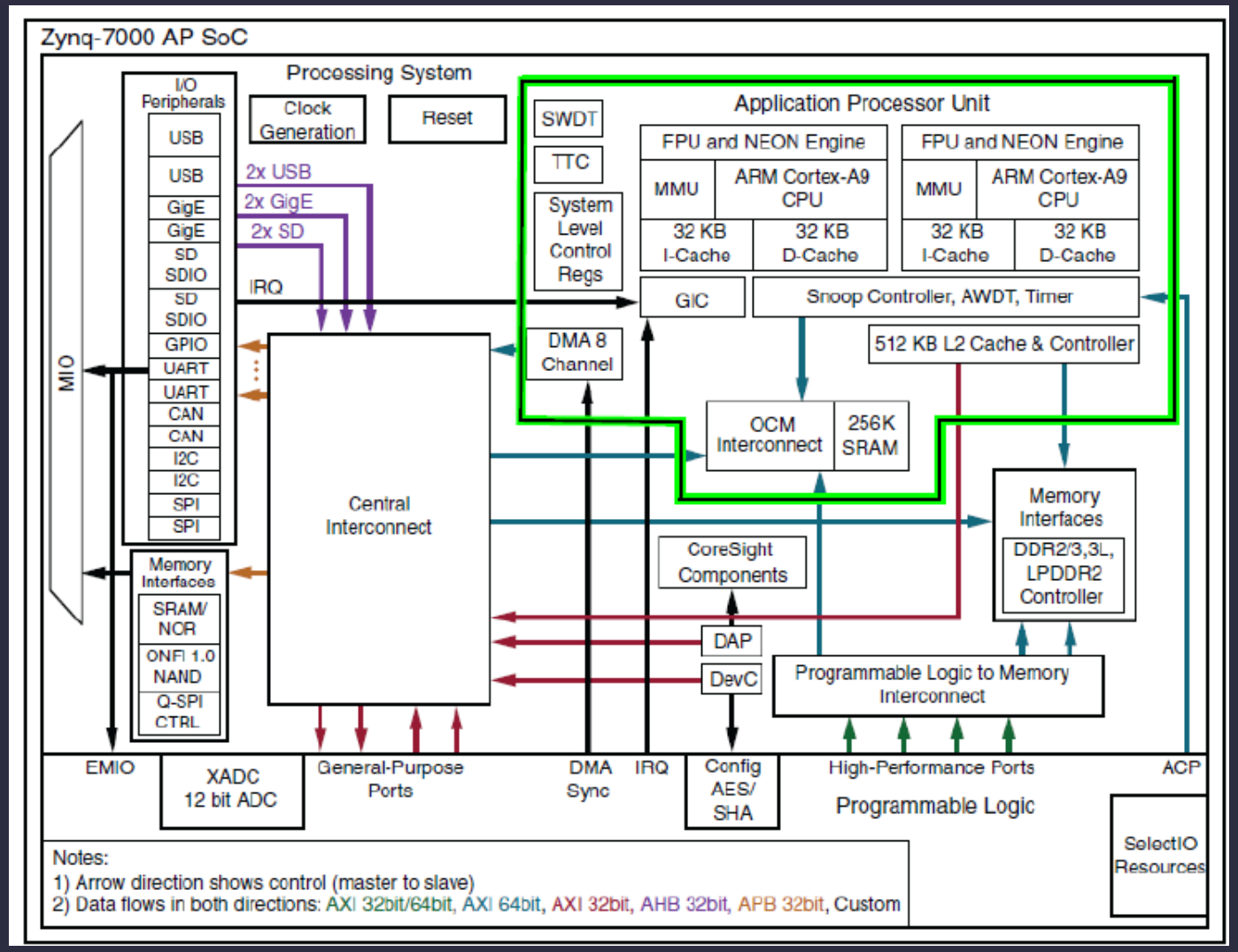
Simplified ZYNQ Architecture

System on Chip (SOC) Design



A SOC Use Case

System on Chip (SOC) Design



ZYNQ Architecture

- **MIO**: Selects which pin the signals in the I/O interface of the Multiplexed I/O APU will be directed to.
- **EMIO**: Extended Multiplexed I/O ensures that the desired interface is directed to the PL section.
- **APU**: It is the part where the core of the processor is located.
- **General Purpose Ports**: It is the recommended port for low speed data transfer.
- **High Performance Ports**: It is the preferred port for high speed data transfer.• IRQ: It is the port that the PL drives to create an interrupt to the processor.
- **ACP**: It has the same features as the HP port. However, it works consistently with the processor's cache (Cache Coherence).