SOC Design

Week 3: ZYNQ Architecture

Fenerbahçe University

Professor & TAs

Prof: Dr. Vecdi Emre Levent

Office: 311

Email: emre.levent@fbu.edu.tr

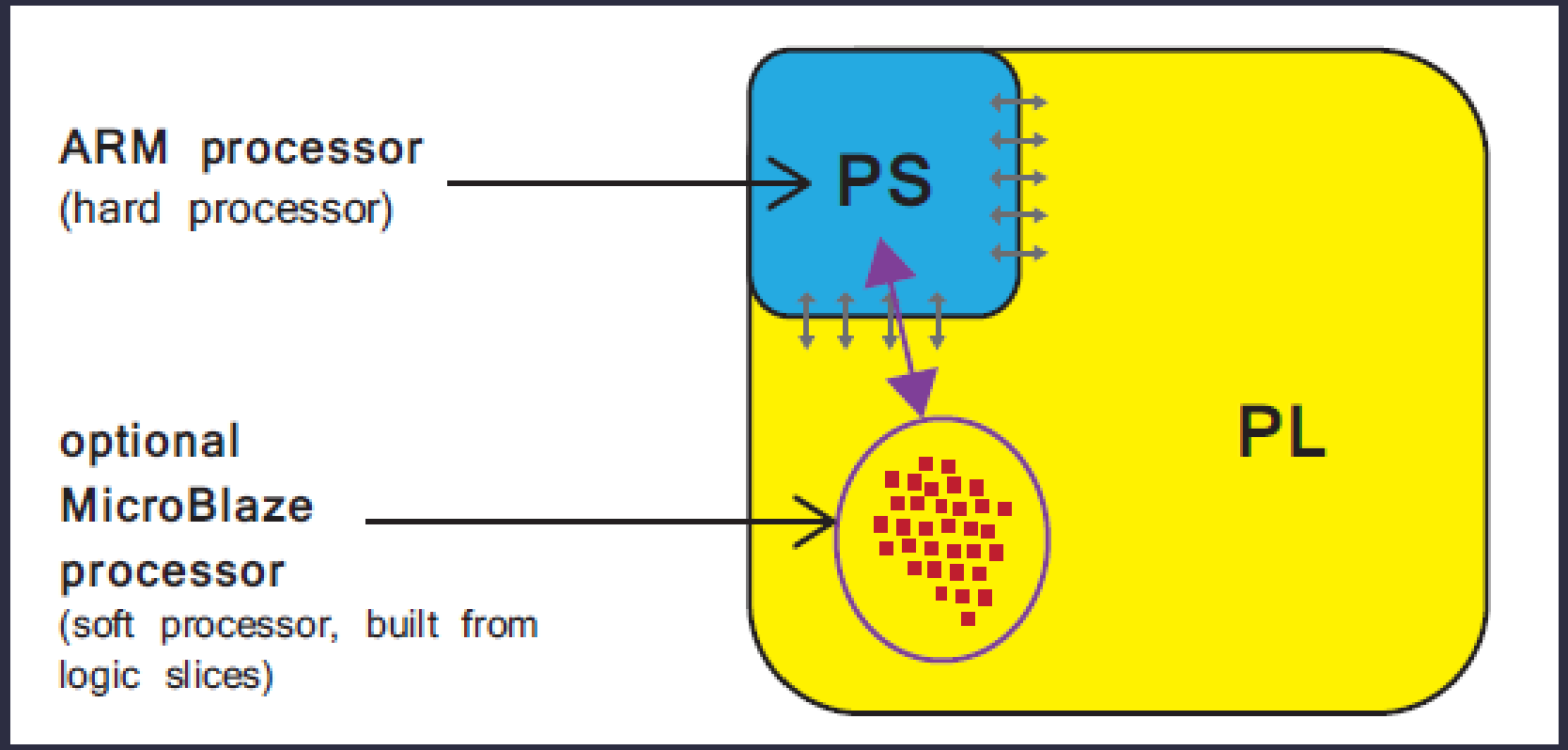
TA: Arş. Gör. Ezgi Çakmak

Office: 311

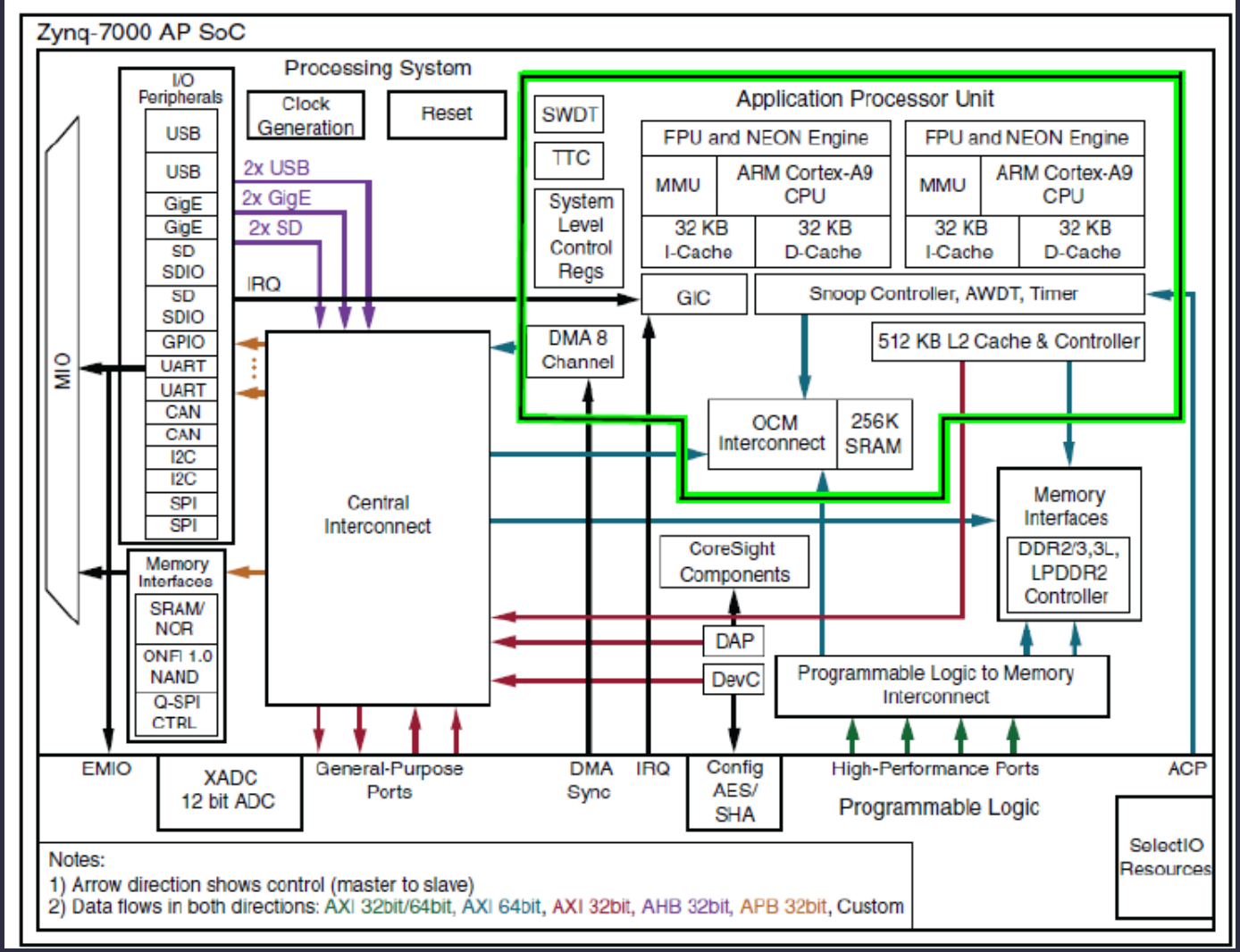
Email: ezgi.cakmak@fbu.edu.tr

ZYNQ Architecture

- ARM Cortex A9
- Softcore Microblaze



ZYNQ Architecture

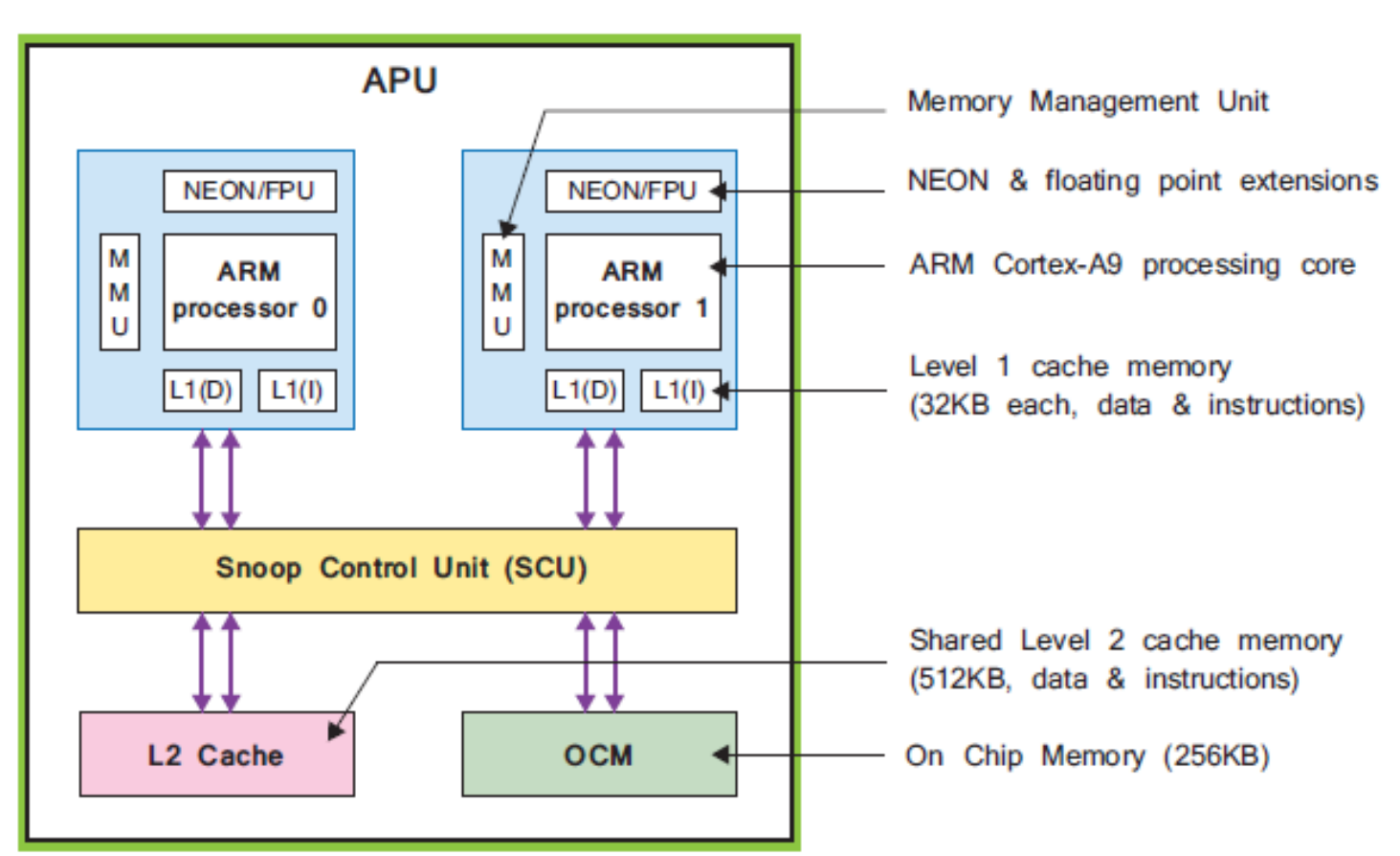


ZYNQ Architecture

- **MIO**: Selects which pin the signals in the I/O interface of the Multiplexed I/O APU will be directed to.
- **EMIO**: Extended Multiplexed I/O ensures that the desired interface is directed to the PL section.
- **APU**: It is the part where the core of the processor is located.
- **General Purpose Ports**: It is the recommended port for low speed data transfer.
- **High Performance Ports**: It is the preferred port for high speed data transfer.• IRQ: It is the port that the PL drives to create an interrupt to the processor.
- **ACP**: It has the same features as the HP port. However, it works consistently with the processor's cache (Cache Coherence).

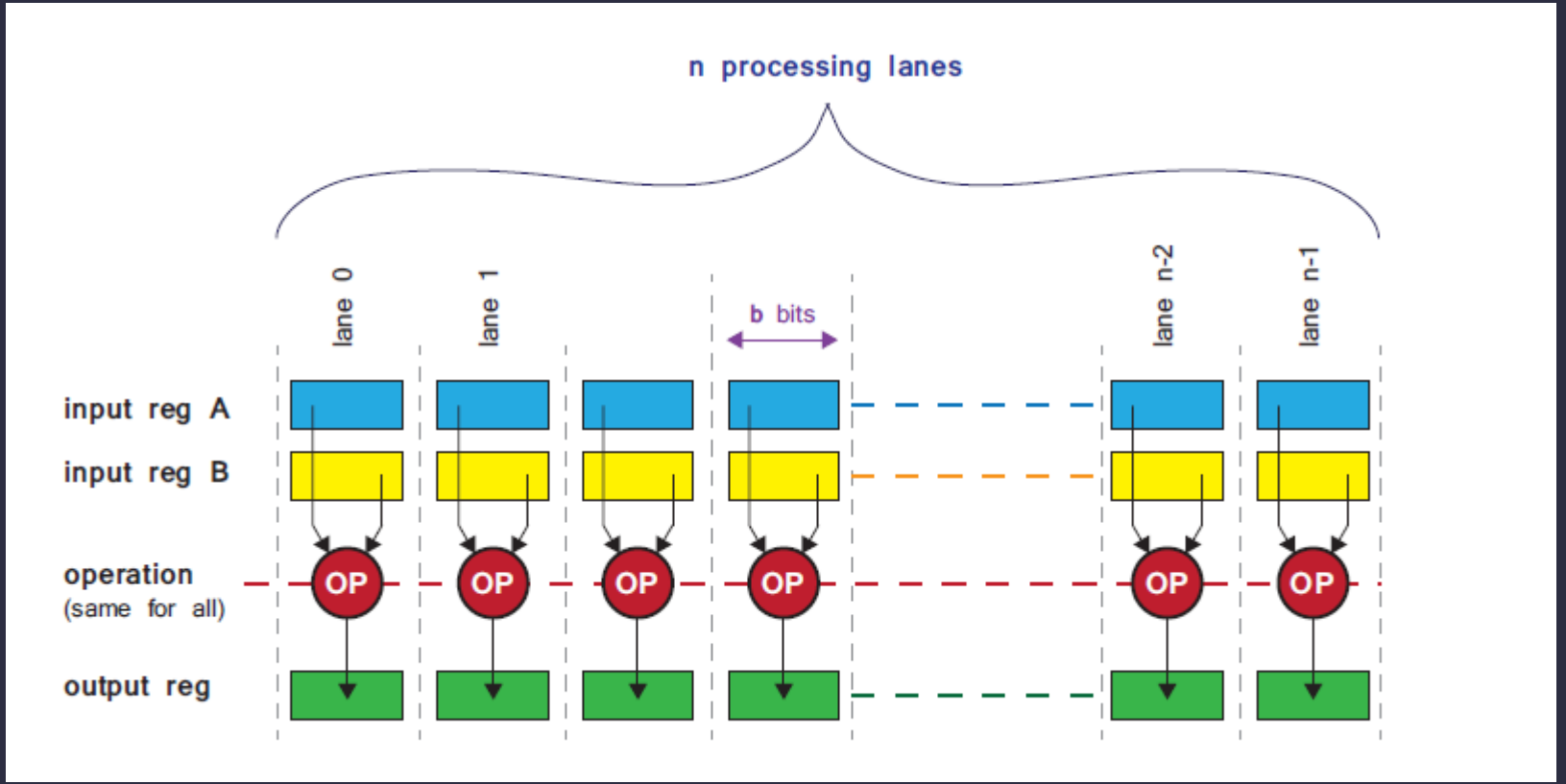
ZYNQ Architecture

- Block diagram of the application processing unit



ZYNQ Architecture

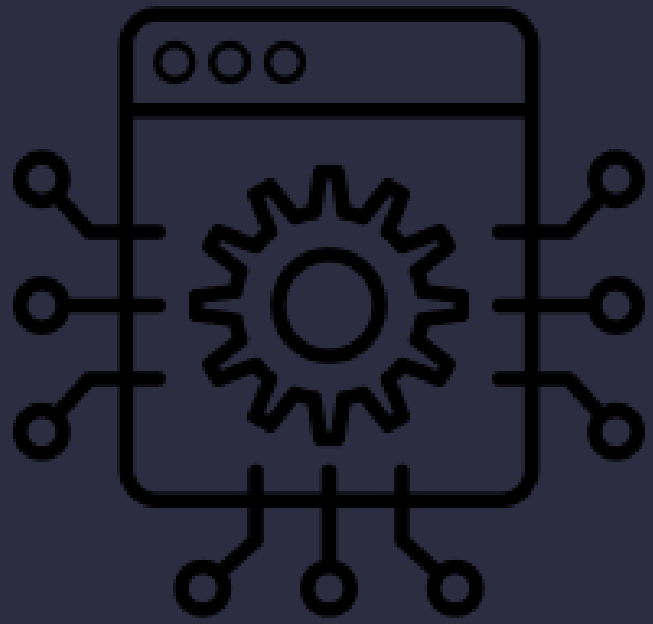
- Single Instruction Multiple Data (SIMD) processing in the NEON MPE



ZYNQ Architecture

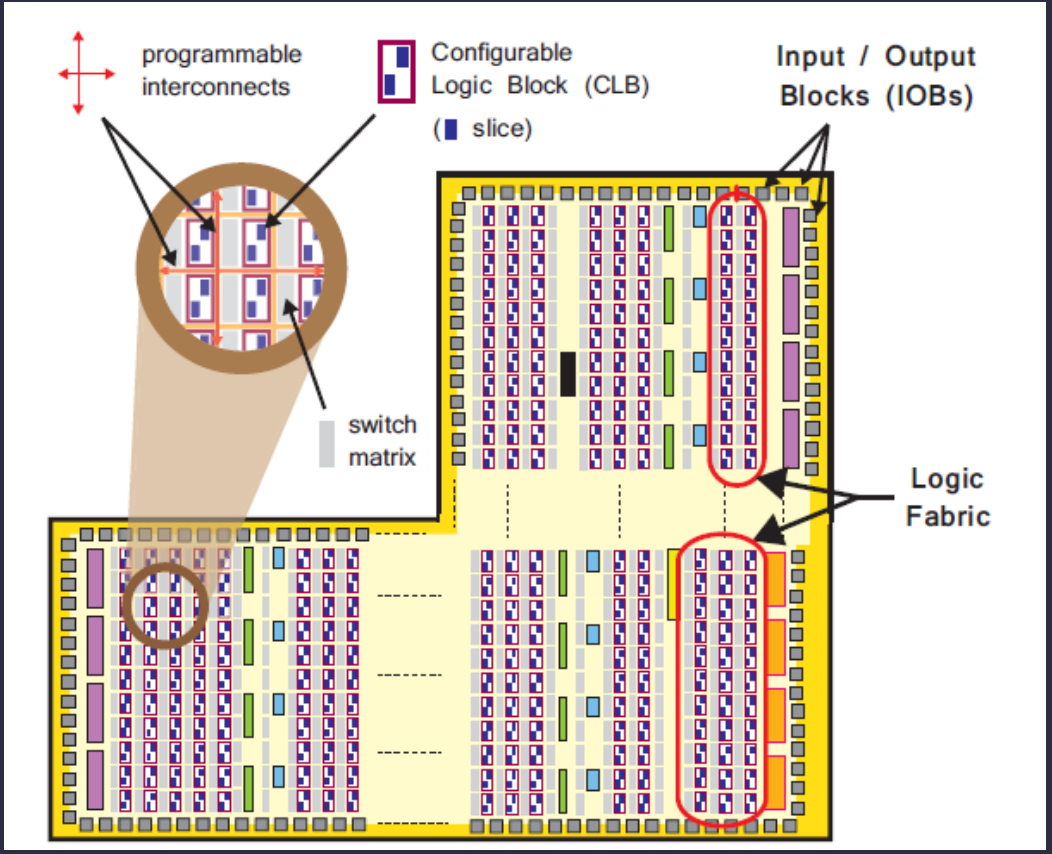
- List of I/O Peripheral Interfaces

  - SPI (x2)
  - I2C (x2)
  - CAN (x2)
  - UART (x2)
  - GPIO
  - SD (x2)
  - USB (x2)
  - GigE (x2)



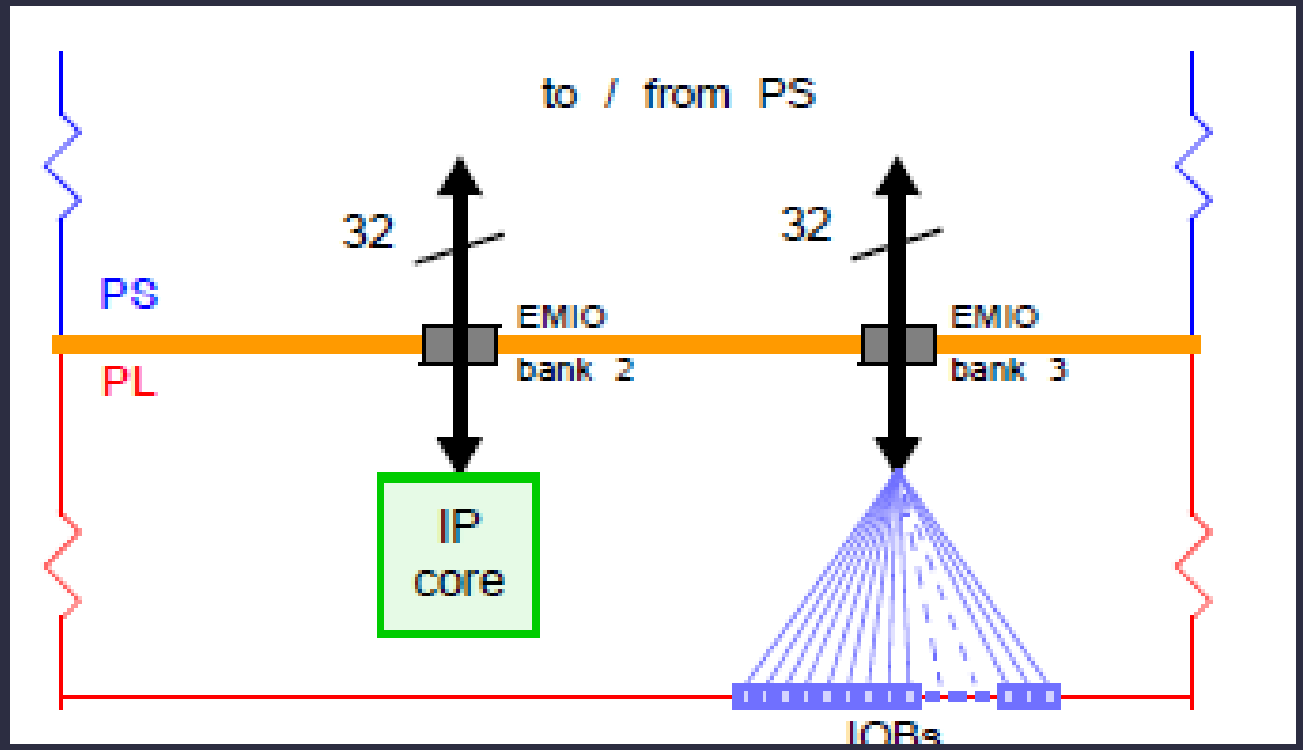
ZYNQ Architecture

- The logic fabric and its constituent elements



ZYNQ Architecture

- Using the EMIO to interface between PS and PL



ZYNQ Architecture

- Interfaces between PS and PL

Interface Name	Interface Description	Master	Slave
M_AXI_GP0	General Purpose (AXI_GP)	PS	PL
M_AXI_GP1		PS	PL
S_AXI_GP0	General Purpose (AXI_GP)	PL	PS
S_AXI_GP1		PL	PS
S_AXI_ACP	Accelerator Coherency Port (ACP), cache coherent transaction	PL	PS
S_AXI_HP0	High Performance Ports (AXI_HP) with read/write FIFOs. (Note that AXI_HP interfaces are sometimes referred to as AXI Fifo Interfaces, or AFIs).	PL	PS
S_AXI_HP1		PL	PS
S_AXI_HP2		PL	PS
S_AXI_HP3		PL	PS

ZYNQ Architecture

- Zynq-7000 family members

	Z-7010	Z-7015	Z-7020	Z-7030	Z-7045	Z-7100
Processor	Dual core ARM Cortex-A9 with NEON and FPU extensions					
Max. processor clock frequency	866MHz			1GHz		
Programmable Logic	Artix-7			Kintex-7		
No. of FlipFlops	35,200	96,400	106,400	157,200	437,200	554,800
No. of 6-input LUTs	17,600	46,200	53,200	78,600	218,600	277,400
No. of 36Kb Block RAMs	60	95	140	265	545	755
No. of DSP48 slices (18x25 bit)	80	160	220	400	900	2020
No. of SelectIO Input/Output Blocks[a]	HR: 100 HP: 0	HR: 150 HP: 0	HR: 200 HP: 0	HR: 100 HP: 150	HR: 212 HP: 150	HR: 250 HP: 150
No. of PCI Express Blocks	-	4	-	4	8	8
No. of serial transceivers	-	4	-	4	8 or 16[b]	16
Serial transceivers maximum rate	-	6.25Gbps	-	6.6Gbps / 12.5Gbps [c]	6.6Gbps / 12.5Gbps [b]	10.3Gbps

ZYNQ Architecture

- General ZYNQ Architecture