

SOC Design

Week 9: Interfaces II



Fenerbahçe University



Professor & TAs

Prof: Dr. Vecdi Emre Levent

Office: 311

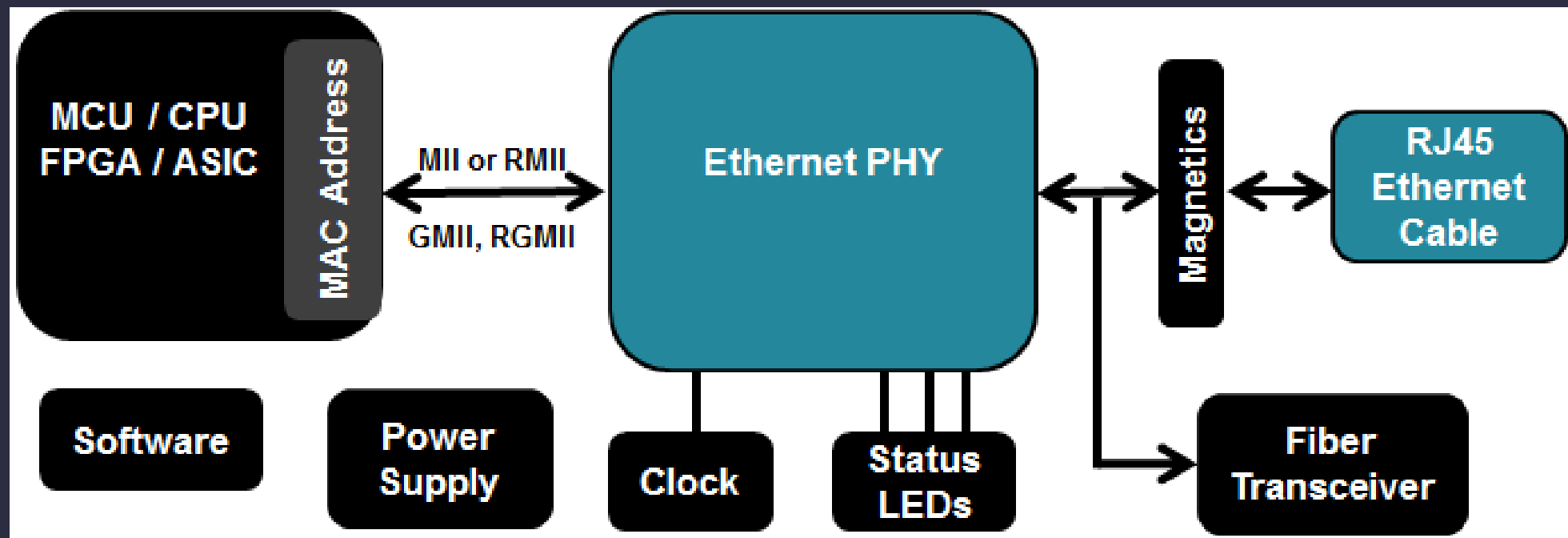
Email: emre.levent@fbu.edu.tr

TA: Arş. Gör. Ezgi Çakmak

Office: 311

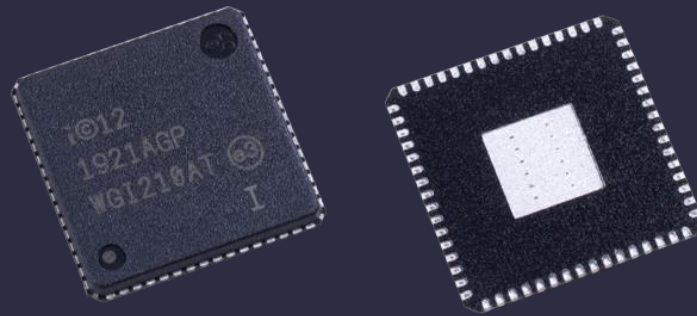
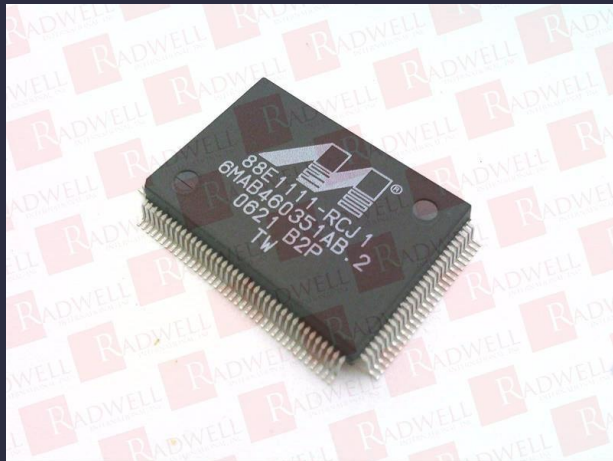
Email: ezgi.cakmak@fbu.edu.tr

Ethernet



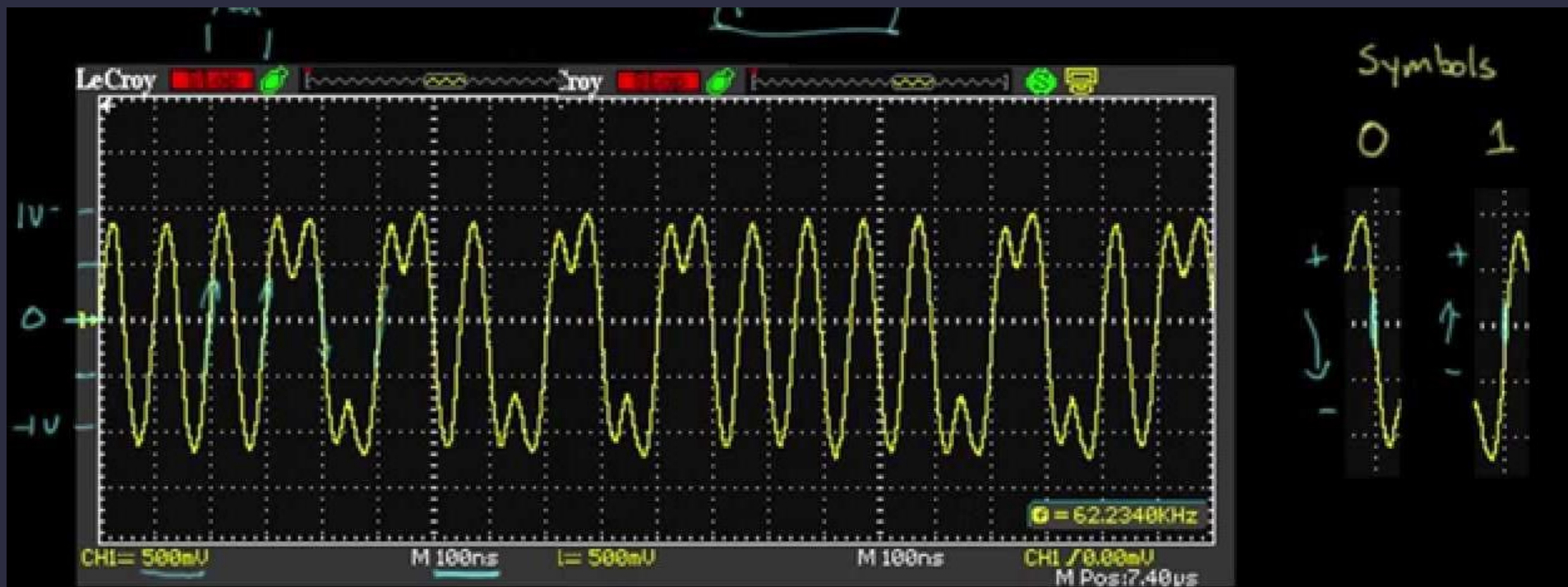
Ethernet PHY – FPGA Connection

Ethernet



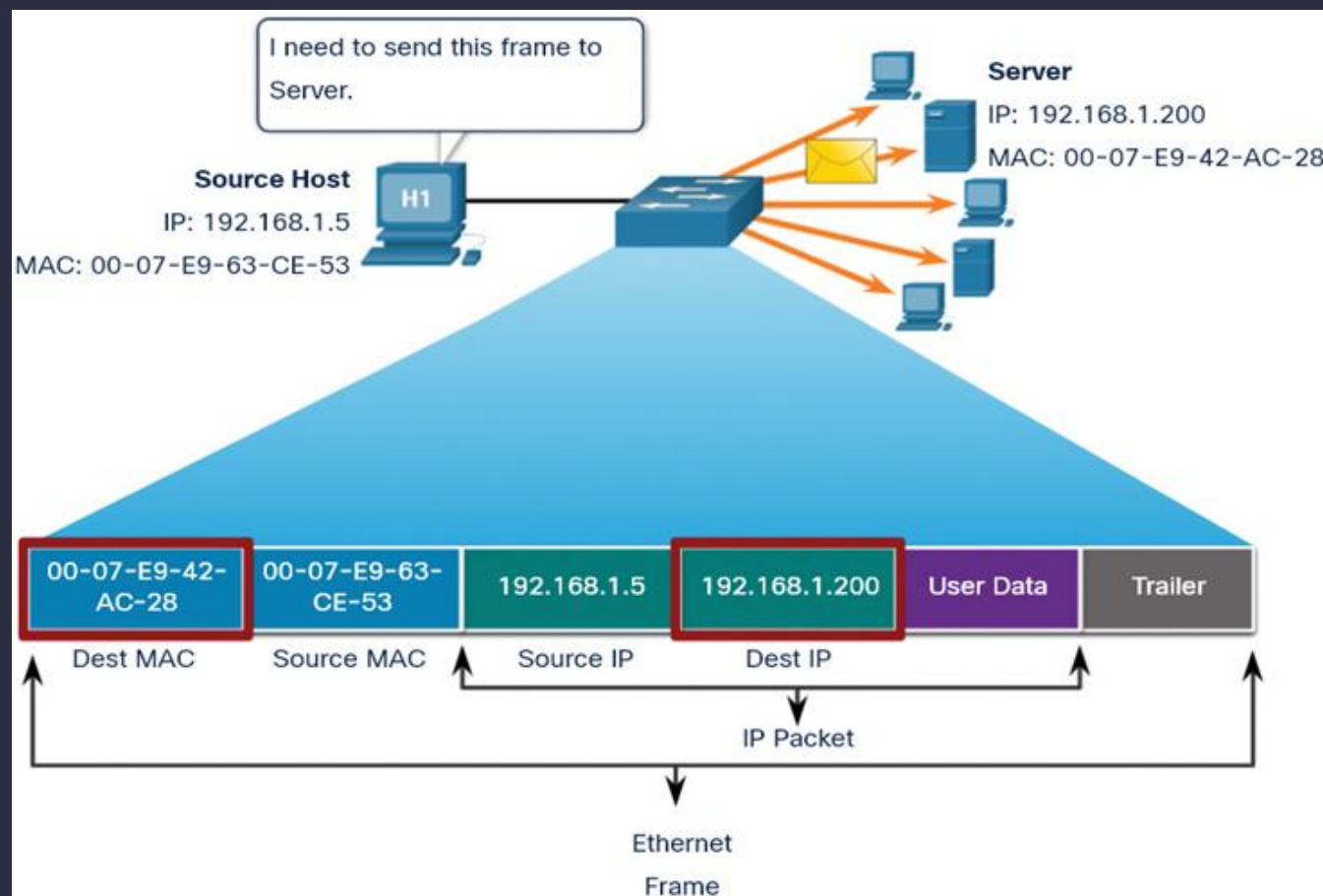
Ethernet PHY ICs

Ethernet



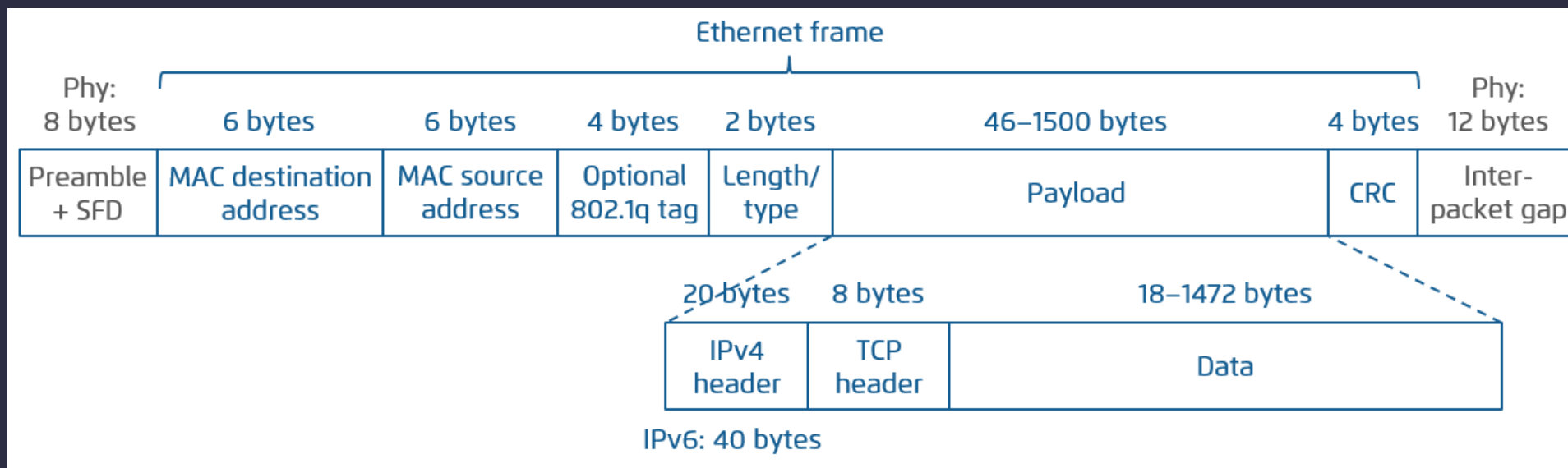
Ethernet Signals

Ethernet



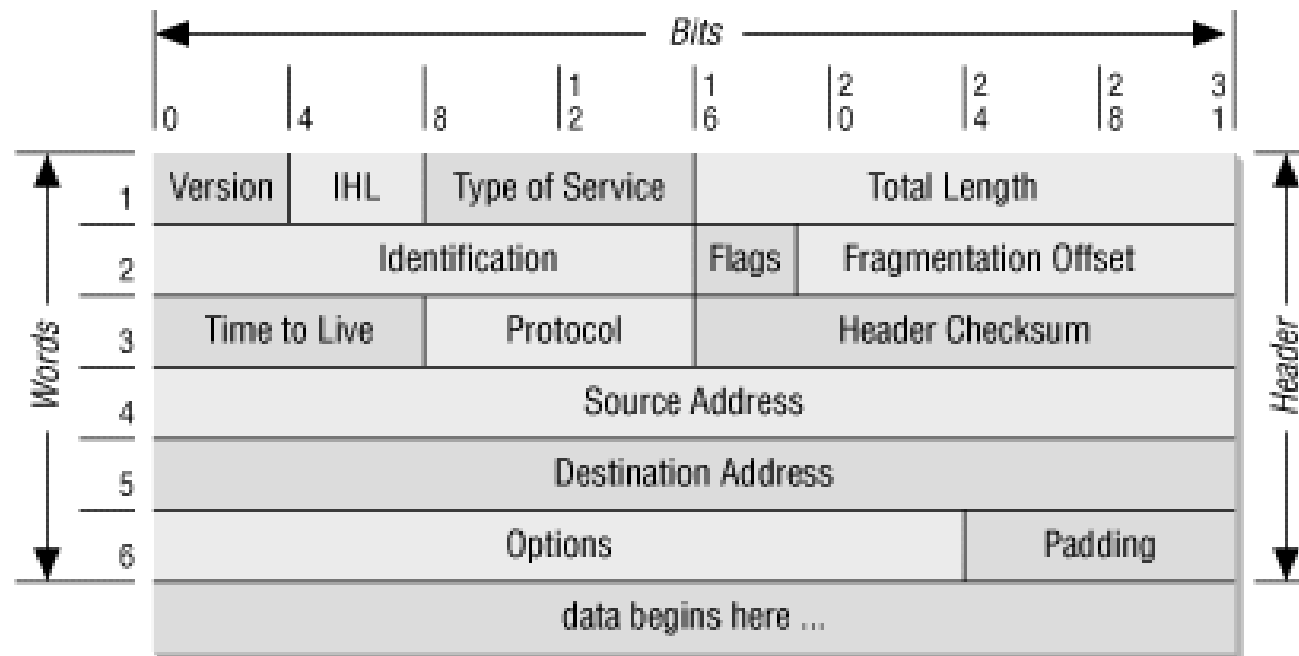
Ethernet MAC Layer Packet

Ethernet



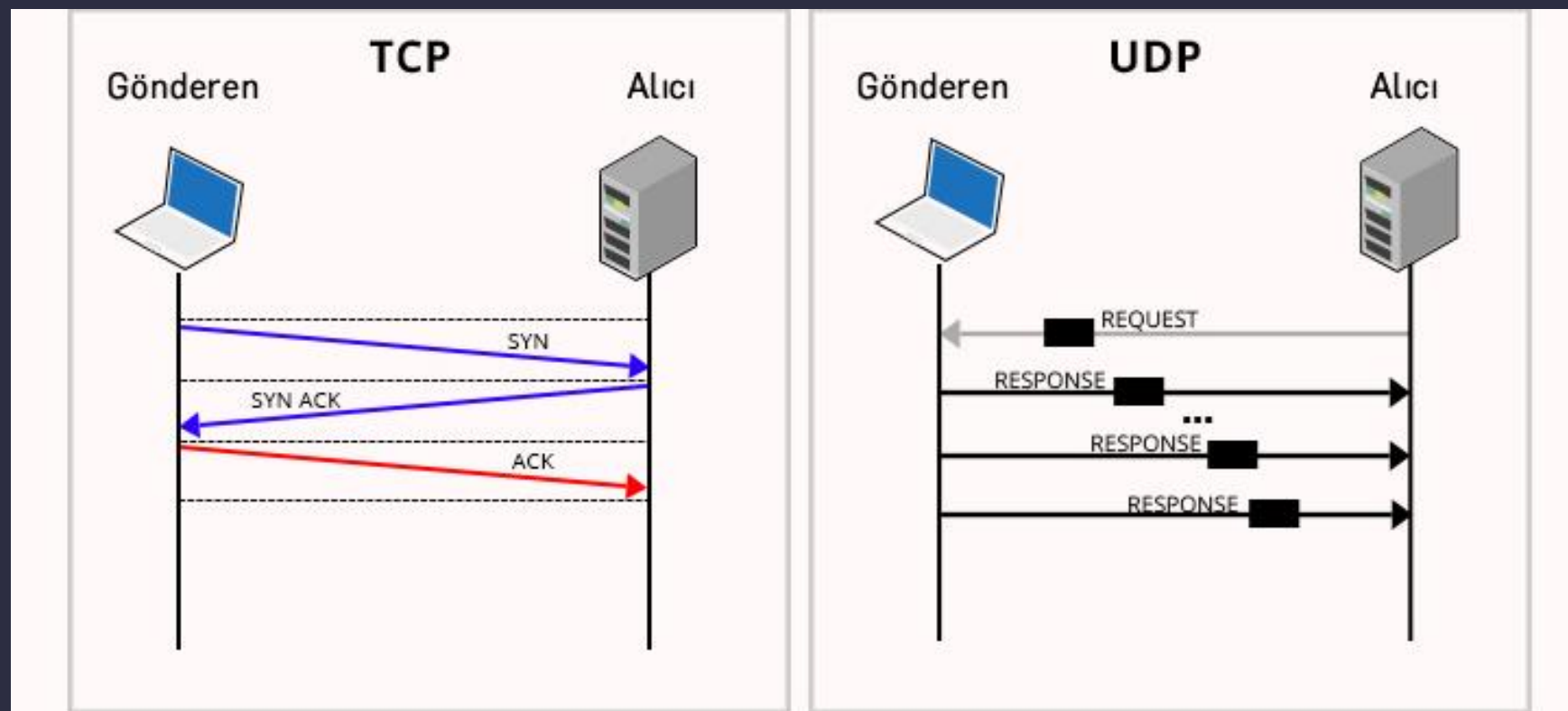
UDP Packet

Ethernet



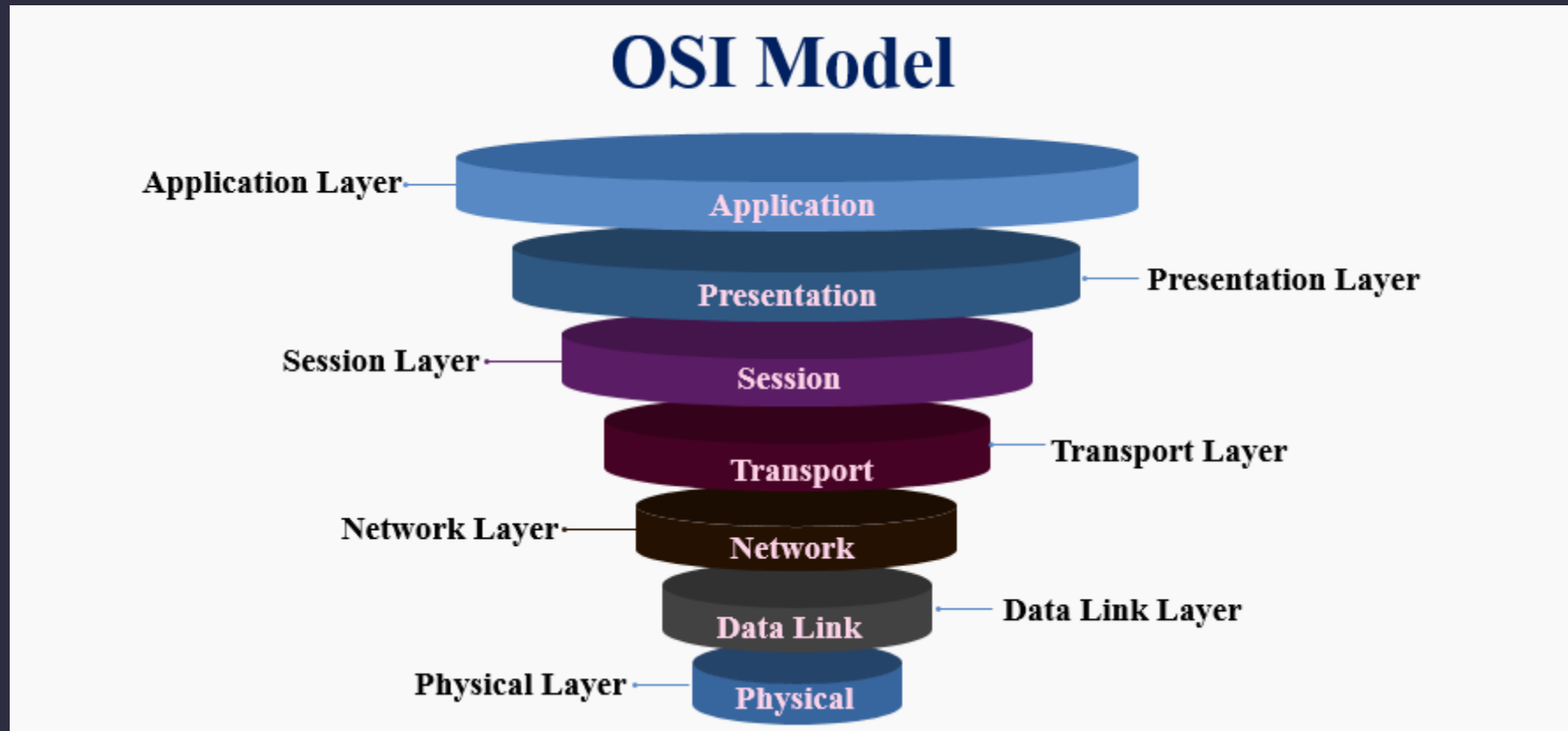
UDP Packet

Ethernet



TCP vs UDP

Ethernet



OSI Layers

Ethernet

No. -	Time	Source	Destination	Protocol	Info
11	1.226156	192.168.0.2	192.168.0.1	TCP	3196 > http [SYN] Seq=0 Len=0 MSS
12	1.227282	192.168.0.1	192.168.0.2	TCP	http > 3196 [SYN, ACK] Seq=0 Ack=
13	1.227325	192.168.0.2	192.168.0.1	TCP	3196 > http [ACK] Seq=1 Ack=1 Win
14	1.227451	192.168.0.2	192.168.0.1	HTTP	SUBSCRIBE /upnp/service/Layer3For
15	1.229309	192.168.0.1	192.168.0.2	TCP	http > 3196 [ACK] Seq=1 Ack=256 W
16	1.232421	192.168.0.1	192.168.0.2	TCP	[TCP Window Update] http > 3196 [
17	1.248355	192.168.0.1	192.168.0.2	TCP	1025 > 5000 [SYN] Seq=0 Len=0 MSS
18	1.248391	192.168.0.2	192.168.0.1	TCP	5000 > 1025 [SYN, ACK] Seq=0 Ack=
19	1.250171	192.168.0.1	192.168.0.2	HTTP	HTTP/1.0 200 OK
20	1.250285	192.168.0.2	192.168.0.1	TCP	3196 > http [FIN, ACK] Seq=256 Ac
21	1.250810	192.168.0.1	192.168.0.2	TCP	http > 3196 [FIN, ACK] Seq=114 Ac
22	1.250842	192.168.0.2	192.168.0.1	TCP	3196 > http [ACK] Seq=257 Ack=115
23	1.251868	192.168.0.1	192.168.0.2	TCP	1025 > 5000 [ACK] Seq=1 Ack=1 Win
24	1.252826	192.168.0.1	192.168.0.2	TCP	http > 3196 [FIN, ACK] Seq=26611
25	1.253323	192.168.0.2	192.168.0.1	TCP	3197 > http [SYN] Seq=0 Len=0 MSS
26	1.254502	192.168.0.1	192.168.0.2	TCP	http > 3197 [SYN, ACK] Seq=0 Ack=
27	1.254532	192.168.0.2	192.168.0.1	TCP	3197 > http [ACK] Seq=1 Ack=1 Win

⊞ Frame 11 (62 bytes on wire, 62 bytes captured)

⊞ Ethernet II, Src: 192.168.0.2 (00:0b:5d:20:cd:02), Dst: Netgear_2d:75:9a (00:09:5b:2d:75:9a)

⊞ Internet Protocol, Src: 192.168.0.2 (192.168.0.2), Dst: 192.168.0.1 (192.168.0.1)

⊞ Transmission Control Protocol, Src Port: 3196 (3196), Dst Port: http (80), Seq: 0, Len: 0


```

0000  00 09 5b 2d 75 9a 00 0b 5d 20 cd 02 08 00 45 00  ..[-u... ] .....E.
0010  00 30 18 48 40 00 80 06 61 2c c0 a8 00 02 c0 a8  .O.H@... a,.....
0020  00 01 0c 7c 00 50 3c 36 95 f8 00 00 00 00 70 02  ...|.P<6 .....p.
0030  fa f0 27 e0 00 00 02 04 05 b4 01 01 04 02     ...'.....
  
```

Wireshark for Sniffing

Ethernet

Board Support Package Settings

Control various settings of your Board Support Package.

Overview

- standalone
 - lwip140
 - xilmfs
- drivers
 - cpu

web_server_bsp

OS Type: *standalone* Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and exceptions as well as the basic features of a hosted environment, such as standard input and output, profiling, abort and exit.

OS Version: 3.11.a

Target Hardware

Hardware Specification: E:\Web_server\SDK\Web_server_hw_platform\system.xml

Processor: microblaze_0

Supported Libraries

Check the box next to the libraries you want included in your Board Support Package. You can configure the library in the navigator on the left.

Name	Version	Description
<input type="checkbox"/> dosfs	1.03.a	Provides FAT12, FAT16 and FAT32 access using simpl...
<input checked="" type="checkbox"/> lwip140	1.06.a	LwIP TCP/IP Stack library: lwIP v1.4.0, Xilinx adapter v...
<input type="checkbox"/> xilfatfs	1.00.a	Provides read/write routines to access files stored on...
<input type="checkbox"/> xilflash	3.04.a	Xilinx Flash library for Intel/AMD CFI compliant paral...
<input type="checkbox"/> xilif	3.02.a	Xilinx In-system and Serial Flash Library
<input checked="" type="checkbox"/> xilmfs	1.00.a	Xilinx Memory File System
<input type="checkbox"/> xilskey	1.01.a	Xilinx Secure Key Library

OK Cancel

Lightweight TCP/IP (lwIP) Stack Xilinx BSP